A THESIS ON

IRON RELATED DEFECTS IN QUENCHED SILICON

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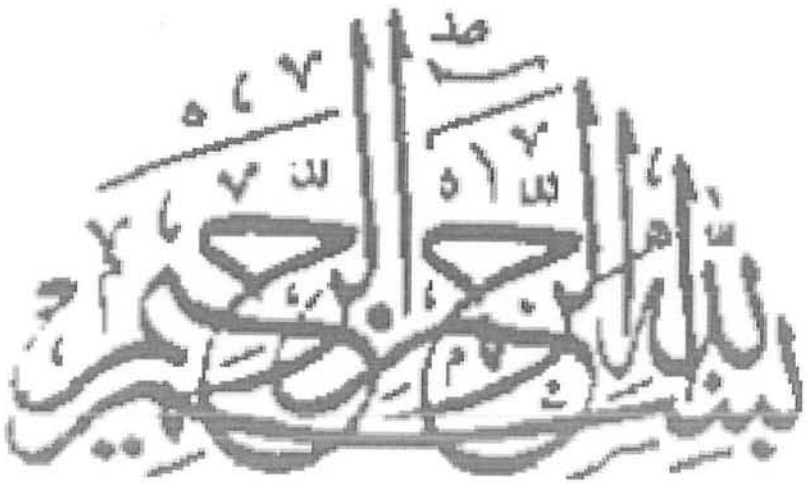
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CERTIFICATE

Certified that the work reported in this thesis has been carried out in Advance Materials Physics Laboratory by **Muhammad Nawaz Saleh** under my supervision.

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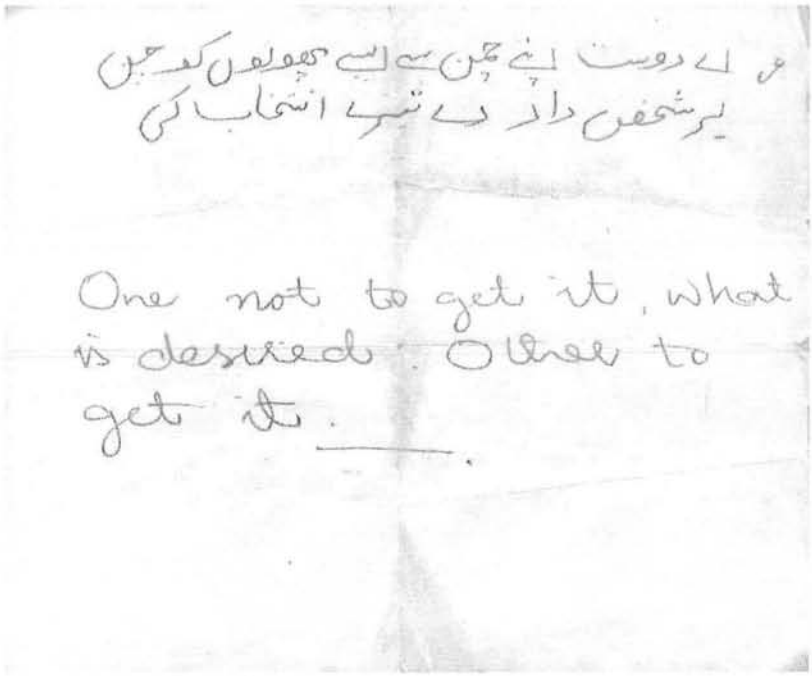
TO

"Beginning of a Love Poem
&
To The End of Fairy Tales"



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Muhammad Nawaz

ABSTRACT

The aim of our research project is to (i) develop a digital computerized DLTS system in the laboratory and (ii) study iron related defects in quenched silicon. In the first part of project, two main IEEE based components, capacitance meter and pulse generator are interfaced with a computer. A software in Visual C++ has been programmed for communication and acquisition of data. Preliminary test run using our DLTS system has been taken to establish the performance of the system. It is found that our system is working well so for as the test run and initial measurements are concerned. However improvement in software and supporting equipment is still needed to enhance and extend its working. In the second part of the project, quenched samples of silicon has been studied in detail using a commercial DLTS system available in the department. At least two deep levels at energies E_c-0.55, and E_c-0.25 eV are observed in high concentration. The annealing characteristics of the two states E_c-0.55 and E_c-0.25 eV were measured. The annealing characteristics of E_c-0.55 gold related acceptor level showed the contribution of signal due to iron in a peak corresponding to energy position E_c- 0.55 eV. The other energy state at E_c-0.25 eV is identified as iron-gold complex. The characteristics of these two defects also suggest that they are pinned together. The comparison of emission rate signatures and annealing characteristics revealed that energy state at E_c-0.55 eV is due to gold acceptor and energy state E_c-0.25 eV is due to iron-gold complex. The inadvertent gold and iron are present in the samples.

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CHAPTER 5

EXPERIMENTAL DETAILS

CHAPTER 1

Introduction

1.1 Introduction

Semiconductors are the most significant materials because the whole modern electronic technology is based on them. Semiconductors are the main focus of research since last fifty years. They are very useful because of their temperature depended electrical conductivity. They overpass the large breach of electrical conductivities between metals and insulators. Their electronic properties can be controlled by applying voltage, magnetic field, light, mechanical stress, and change in temperature [1].

Today the modern semiconductor electronic devices are playing an important role in almost every field of life extending from domestic appliances to the sophisticated devices used in defense and space technology. Developments in the device technology have brought revolution in the field of high speed communication, computation, microminiaturization of integrated circuitry and fabrication of the novel nanostructures. An increasing variety of materials is being used to produce semiconducting devices to perform specific device functions. Considerable efforts are being made to increase efficiency and to reduce the dimensions of the devices to produce

low cost devices. Silicon, because of its great abundance in earth's crust and many useful properties, is still dominantly the material of choice in the semiconductor industry.

Crystal defects play a predominant role in controlling the most interesting properties of semiconductors. As donors and acceptors, they find out the electronic properties of the semiconducting material. Defects in semiconductors have retained a central role, from the invention of the transistor to the current generation of microelectronic devices and circuits. The central role, adverse or beneficial, has been the main thrust in advancing methods and techniques for the understanding of the origin of defects, their characteristics and influence on device performance. Thus, the remarkable advances in solid state electronic science and technology are to a large extent directly attributable to the role of defects in semiconductors. Similarly, the function of electronic devices which manipulate, amplify, switch and control currents, voltages, process and store information, is essentially based on the transition of electron from one energy state to other which are due to controlled introduction of defects in semiconductor crystal.

1.2 Classification of Defects in Semiconductors.

Impurities and structural defects in semiconductor crystals introduce energy states within the forbidden energy gap. If an atom of host lattice is replaced by a different atom that belongs to some other group of the period table, it changes the periodic potential of the crystal and the wave function at that site. New electronic states are produced by such a defect whose energy may lie within the band gap. These levels can be classified into the following two categories depending upon the depth of the energy level corresponding to the ground state of the impurity with respect to the nearest band edge.

- Shallow level defects
- Deep-level defects

1.2.1 Shallow level Defects

The defects states produced in the band gap closer to either the conduction or the valence band edges are named as shallow level defects. If the wave function describing

the defect state in the band structure of the host crystal is delocalized in real space, the state is known as shallow level [2-3].

Shallow levels have small binding energies (typically << 0.1eV). Shallow levels act as either donors or acceptors and contribute electrons or holes respectively. They determine the conduction properties of the semiconductors and are mostly ionized at room temperature. When impurities from group IIIA and group VA of the periodic table are introduced into group IVA elements then energy levels close to the valence- and conduction-band edges are produced.

1.2.2 Deep-Level Defects.

If the binding energy of the defects is large than shallow levels from the nearest band edge, it is called a deep level and the defect is termed as a deep level defects. If the wave function is localized in real space the defect state introduces a deep level [2-3]. The importance of the deep level defects lies in their property to act as a mediating step within the band gap during the transition of electrons and holes and hence to control their lifetime. They are commonly caused by impurities, device processing steps and irradiation with high energy particles. For example, impurities from groups other than III and V of the periodic table such as copper, iron, and gold etc. introduce energy levels nearer to the middle of the forbidden energy gap. Deep-levels defects have enormous impact on the performance of electronic devices and play a key role in controlling the minority carrier-life time.

1.3 Motivation of Present Work.

Tremendous and enormous progress in silicon technology has motivated me to investigate the iron contamination in silicon materials. This marvelous advancement in silicon technology has become only possible because of the reduction of iron contamination during the growth processes of the device. The Semiconductor Industry Association (SIA) International Technology Roadmap specified 1.4×10^{10} cm^{-2} as the maximum allowable surface iron contamination in the year 2000, decreasing to 5×10^{9}

cm^{-2} of iron in 2005 [1]. These low levels of acceptable contamination require ultra pure environment on all steps of the technological process for the dedicated devices.

Iron is certainly one of the most troubling contaminants in the IC industry. Iron is a very common element in nature, and is difficult to completely eliminate on a production line. Therefore, the unintentional iron contamination level in wafer is higher than that of other metal impurities [4].

Iron related defects have been studied in iron-doped samples at different temperatures under different reverse voltages.

DLTS technique is the only electrical technique that can measure electrically active defects down one part in billion. It therefore, inspired me to work on DLTS system for getting a comprehensive picture of the system design. The main purpose of the this project was to develop a Digital Computerized Deep Level Transient Spectroscopy (DLTS) system in our Advance Materials Physics Laboratory (AMPLAB) thereby attaining a comprehensive understanding of hardwaring, softwaring and its different operational features. The shipment of the parts was not done in time. In spite of this, system is developed with little resources in limited time. Improvements and extensions to its present capabilities are possible.

1.4 Scheme of Thesis

Chapter 2 included the historical background on the different defect states associated with different transition metals (TM) e.g Ag, Au and Fe, their complexes with intrinsic defects. It provides the information about different characteristics of these defects, like capture cross-section, activation energy, emission rates, and defect concentration. This chapter also included the history of quenched-in defects, especially those associated with iron. The complexes of iron with boron or other impurities and its defect states whether stable, unstable or metastable are also studied.

In chapter 3 a brief description of current-voltage and capacitance-voltage characteristics, single-shot technique and Deep Level Transient Spectroscopy (DLTS) is studied. The principle and theory of the DLTS is discussed. Chapter 4 deals with the development of DLTS. Hardware is explained in detail in this chapter. Interfacing of the

devices with PC through GPIB cards is configured. Coupling circuit is designed, assembled, and interfaced for pulses width of nanosecond. To communicate with all these devices for measurements, a software in Visual C++ has been programmed.

The final chapter 5 explains the experimental details including the electrical measurements, single shot and deep level transient spectroscopy measurements. The results are discussed and compared with literature. Possibilities of enhancement of digital computerized DLTS system are discussed.

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CHAPTER

2

Historical Review of Iron-related Defects in Silicon

2.1 Introduction

Invention of transistor has made tremendous progress in silicon technology. Device performance has been improved by at least a factor of a million in every respect. The number of transistors per chip has increased to 200 million for 256 MB DRAM and 20 million for microprocessor. This became only possible because the growth of device is controlled in sense of defects and impurities related to iron and other elements contamination. The Semiconductor Industry Association (SIA) International Technology Roadmap specified $1.4x10^{10}$ cm^{-2} as the maximum allowable surface iron contamination in the year 2000 and targeted to decrease to $5x10^{9}$ cm^{-2} of iron in 2005 [1]. Iron is certainly one of the most troubling contaminants in IC industry. Iron is fast diffuser in silicon as compare to other transition metals (TM). Iron is very common element in nature, and is difficult to completely eliminate on production line. Therefore, the unintentional iron contamination level in wafer is usually higher than that of other metal impurities [2]. So iron contamination is detrimental to performance of silicon devices.

Research has been carried out on the fundamental physical properties of iron, impact of iron on device performance, possible sources of iron contamination in production line,

and the reaction paths of iron in silicon wafer during growth of device. A review is written about iron-related isolated and complex defects, concentration of iron on surface and in bulk of silicon.

2.2 Brief History:

In 1957, C.B. Collins and R.O. Carlson studied the iron contamination in silicon. They observed that iron introduced a donor level at 0.40 eV from the valance band in melts and diffused doped p-type silicon at 1200 ^{0}C. This level converts anomalously to a level at 0.55 eV from conduction band at room temperature. This conversion occurs in the order of a month at room temperature and speeds up to about 5 hours at 50 ^{0}C. The conversion is reversible in range from 70 ^{0}C ~200 ^{0}C. Above 200 ^{0}C, the iron has precipitated in the volume or at the sample surfaces [3]. No accepter level is observed. The electrically active solubility of iron, $1.5x10^{16}$ cm^{-3} at 1200 ^{0}C, is higher than the radiotracer solubility because sample was rapidly quenched in water.

Woodbury and Ludwig (1960) [4], measured the solubility of iron in silicon. Maximum solubility of iron in silicon was $1.5x10^{16}$ cm^{-3}. Donor level was at E_V+0.40eV. They observed the unchanged resistivity on the diffusion of iron in n-type silicon

In 1964, Bemski and Dias quenched p-type silicon from 600 ^{0}C ~800 ^{0}C to room temperature. They measured that bulk resistivity increased with increasing temperature. They also measured that donor concentration had increased with increasing temperature. They observed a stable donor level at E_v+0.40 eV [5].

In 1967, Elstner and Kamprath obtained same results as Bemski using same resistivity measurements technique [6].

In 1974, Yau and Sah measured two levels at E_c-0.264 eV and E_c-0.54 eV in gap of silicon [7]. Iron diffused silicon p-n junctions were heat treated at elevated temperature for long time and quenched to room temperature. They measured that Phosphorous gettering could not remove these defects but slow quenching did so. They suggested that these deep levels were associated with the same iron center.

In 1977, J.D. Gerson, L.J. Cheng, and J.W. Corbett, reported that fast cooling or quenching creates defects in silicon crystals. They pointed out that silicon crystals contains many impurities as found by chemical and physical analysis [8]. Most of these

defects are electrically inactive or in precipitates in crystal at room temperature. But at elevated temperatures, these precipitates become active and dispersed into crystals. Quenching to room temperature prevents from the precipitation. It was observed by Lee et al [9] by using an EPR spectroscopy for quenched silicon that iron (Fe^0) exits in silicon at interstitial sides. He observed that iron was present in as grown silicon and moved to the T_d interstitial site on heat treatment. They studied majority carrier trapping level in p-type silicon by deep level transient spectroscopy (DLTS) [10]. They used boron–doped polished wafers of float zone (FZ) crystals of 1-, 4-, 10-, and 100-Ωcm resistivities and Czochralski (CZ) crystals of 2- and 10-Ω cm resistivities. They were heated from 900-1200 ^{0}C in atmosphere of nitrogen for 1h and then cooled to room temperature at a cooling rate of ~10^3 ^{0}C/min. DLTS measurements were taken and two defects located at E_v+0.45 and E_v+0.48 eV were found with majority-carrier capture cross-sections $4x10^{-18}$ and $2x10^{-16}$ cm^2 respectively. They found the activation energy for the formation of the E_v+0.45 eV level to be 2.8±0.04 eV which is comparable with the value obtained by Lee et al [11] and Swanson [12].

In 1983, L.C. Kimerling and J.L. Benton studied the interstitial iron substitutional boron pair (Fe_i-B_s) and, association and dissociation reactions in silicon by capacitance transient techniques. The samples were consisted of p-type, <100>, (FZ) and boron doped (10^{13}-10^{16} cm^{-3}) silicon. Iron was introduced into silicon by scraping a wire on both surfaces and then rapid thermal annealing at 1200 ^{0}C for 5 second in flowing argon ambient. Schottky diodes were constructed by evaporating Ti at room temperature. In p-type material the boron related acceptor level at E_v+0.45 eV and interstitial iron donor level at E_v+0.39 eV were observed. The latter was observed by applying reverse bias. It is found that the pair is a simple association of two point charges; the defects are perturbed by minority carrier injection in such away that the boron acceptor level moves toward valence band and the interstitial iron donor level toward conduction band. Above 77 k the dissociation reaction can be driven to almost completion by injection of minority carriers while association process retarded [13].

In 1983, S.D. Brotherton, P. Bradley, A. Gill and B.R. Weber used Electron Para Magnetic Resonance (EPR), diode capacitance measurements and deep level transient spectroscopy (DLTS) to identify the levels in silicon associated with the Au-Fe complex. They found two levels at E_c-0.354 eV and E_v+0.434 eV. Low-temperature annealing confirmed them as the gold-related complex. They used two sets of samples. A-type samples were for EPR and DLTS and B-type for electrical measurements. A-type was (FZ) n-silicon doped with $7x10^{15}$ Phosphorus atom /cm^3. Gold was diffused for 1 to 10h at 1100 ^{0}C and rapid quenched to room temperature. EPR revealed the presence of the Au-Fe complex indicating iron contamination during diffusion [14]. The type B samples were p^+n and n^+p diodes. The n-type diode was fabricated on 102-Ω-cm (FZ). This sample was implanted with 10^{14} iron ions /cm^2 at 180keV for 30 min at 1000 ^{0}C. Gold was diffused from an evaporated film on the rear face for 30 min at 800 ^{0}C and then rapidly quenched to room temperature. The n^+p diode was fabricated on 66-125 Ω-cm (FZ). A thin film of iron was evaporated onto the back face for 30 min at 900^{0}C followed by rapid quench to room temperature.

Indusekhar and V. Kumar (1986) [15], used TSCAN and DLTS and observed two levels at E_v+0.42 eV and E_c-0.52 eV in p-type silicon. They observed that these defects were thermally induced. The source of contamination was quartz tubes and heater filaments at elevated temperature. They noted that E_v+0.42 eV was a complex centre.

In 1987, N. Balasubramanyam and V. Kumar observed that thermal processes such as fast cooling or quenching from elevated temperature can create defects in p-type silicon. These defects are due to iron introduced during various steps of device processing. A hole trap is observed at E_v+0.4 eV in quenched p-type silicon. They observed two levels at E_c-0.54 and E_c-0.29 eV in quenched n-type silicon. The capture cross section of such deep level is ($1.0x10^{-15}$ cm^2) lager than shallow level of order 10^{-16} cm^2 and has a T^{-2} dependence. The samples were epitaxial silicon of thickness 10μm formed on highly doped n-typed silicon. Layer of oxide is grown on the n-Si layer by dry oxidation at 1160 ^{0}C in a quartz tube for 90 min. DLTS was used to take measurements [16].

Hiroshi Nakashima, Takashi Isobe, Yuhide Yamamoto and Kimio Hashimoto in 1988, observed the diffusion coefficient (D_{Fe}=3.3x10^{-1}exp (-0.81/KT)cm^2/s) of iron in silicon wafer. These wafers were p-type F.Z (111) with a boron concentration of 1.2x10^{15} cm^{-3} at room temperature in the range between 0 and 70 ^{0}C. The iron deposited wafer was heat-treated between 950 ^{0}C and 1057 ^{0}C in vacuum for 1.5 to 2.5h and then quenched into liquid nitrogen. DLTS spectra of sample diffused with iron for 4h showed two peaks at around 70 K and 240 K. The thermal emission activation energies of the hole traps were 0.10±0.01 eV and 0.45±0.02 eV from the T^2 correction of the emission rates [17].

In 1989, Kakishta et al, observed three deep levels at E_c-0.21, E_c-0.36 and E_c-0.08 eV in iron-doped silicon by DLTS. They observed that these defects are mobile during storage at room temperature. The origin of these levels is iron-related complexes in silicon [18].

In 1992, H. Nakashima et al, studied metastable iron-boron pairs in p-type silicon by using DTLS, TSCAN, and single shot techniques with minority–carrier injection. Two levels at E_v+0.53 and E_v+0.48 eV are observed as the metastable pairs after the injection at 150 K. The level at E_v+0.53 eV consisted of two traps which vanish with different decay rates at around 220 K but the level at E_v+0.48 eV annihilates with simple exponent ional form [19].

In 1993, H. Nakashima et al [20], measured metastable Fe_i-B_s pair in silicon using dark or photo capacitance transient technique combined with minority carrier injection below 200 K. Five levels at E_c-0.43, 0.46, 0.52, 0.54 and E_v+0.53 eV were observed. They noted that levels at E_c-0.43 eV, E_v+0.53 eV and E_c-0.54 eV were originated from $Fe_i^{+/-}$ that appeared at 2nd, 3rd,and 4th nearest T_d sites adjacent to B_s^- respectively.

In 1995, Shuji Tanaka and Hajime Kitagawa observed that iron introduced a donor level at E_c-0.4 eV with several acceptor levels [21]. It means that positively and negatively charged iron states coexist in n-type silicon. They used phosphorus-doped n-

type, FZ and dislocation-free silicon crystals. The temperature and time of the diffusion ranged from 1130 ^{0}C to 1190 ^{0}C and 30 min to1h respectively followed by rapid quenching into liquid nitrogen. They used DLTS and steady state capacitance technique for this sample. They observed that donor concentration decays during storage at room temperature.

In 1997, T. Sadoh et al, noted two deep levels in n-type silicon using thermally stimulated capacitance technique (TSCAP) combined with minority carrier injection. These levels were at E_v+0.31 and E_v+0.41 eV. The level at E_v+0.41 eV is due to interstitial iron and first one is due to complex of interstitial and hydrogen. The sample was annealed at 175 ^{0}C for 30 min. They noted that transition metals such as vanadium [22], chromium [23], and iron tend to form complexes with hydrogen in n-type silicon. These complexes induce donor levels below the donor levels of the isolated interstitial species.

In 1998, Shuji Tanaka et al observed that the diffusion and electrical characteristics of iron in n-type silicon are less established than those in p-types silicon [24]. They used DLTS and Hall Effect measurement techniques and observed that only a small fraction of iron atoms dissolved can be ionized. They also observed that iron-related defects in CZ-grown n-type silicon were identical to those in floating zone (FZ)-grown n-type silicon. Samples were phosphorus-doped dislocation-free, FZ- and CZ-n-type silicon. The phosphorus concentration in these samples was found $4x10^{13}$ to $4x10^{14}$ cm^{-3}. The samples were divided into smaller slices. Iron was deposited on both the surfaces of the slice by vacuum evaporation.

In 2004, Daniel Macdonald et al, used Deep Level Transient Spectroscopy (DLTS) technique and observed that the interstitial iron (Fe_i) produced deep level in the band gap which had larger capture cross section than holes [25]. According to the Shockley-Read-Hall (SRH) model, the low-injection carrier lifetime should be much lower in p-type silicon (p-Si) than in n-type (n-Si). The recombination strength of a given impurity is determined by three parameters: the energy level and the capture cross sections for both electrons and holes. The iron-doped sample were prepared by ion implantation with dose of 10^{11} cm^{-2} and annealed at 900 ^{0} C for 1h. The float-zone (FZ)

n-si samples of resistivity 2-Ω cm (N_D =2.4x10^{15} cm^{-3}) and 260 μm thickness and p-si (FZ) wafer of 5-Ω cm (N_A=2.8x10^{15} cm^{-3}) and 290 μm thickness were used.

In 2004, L.J. Geerligs and Daniel Macdonald investigated the dynamics of light-induced dissociation of iron-boron (FeB) pairs in p-type silicon. They observed that dissociation was single-exponential process which was balanced with thermal repairing. The dissociation rate is proportional to the square of the carrier generation rate and the inverse square of the FeB concentration. This shows that the dissociation process involves the two recombination or electron capture events. The float-zone (FZ) samples were contaminated with Fe by implantation or diffusion. They used quasi-steady-state photo conductance (QSSPC) to measure the carrier life time [26].

The review reveals that a lot of research has been done on iron contamination, defect levels, and iron concentration under different parameters in silicon. In spite of this research, some ambiguities and controversies still exist. So some aspects need further investigations especially the formation of stable defects in one kind of samples and unstable in other kind of samples.

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CHAPTER

3

Physics of P^+n Junction & Electrical Techniques

This chapter explains the theoretical aspects of p-n junction and it characteristics. Current-voltage characteristics, capacitance-voltage characteristics, single shot transient technique, and deep level transient spectroscopy (DLTS) are explained in detailed.

3.1 Current-Voltage (I-V) Characteristics

The most important property of p-n junction diode is its ability to offer very little resistance to the current flow in the forward bias direction and maximum resistance to the current when reverse biased. Transition region or depletion region of the p-n junction changes with varying applied voltage. When diode is reversed bias the depletion region increases. The only charge carriers able to support a net current across the p-n junction are the minority carriers and hence the reverse current is very small. A forward-biased diode has a decreased depletion region; the majority carriers can diffuse across the junction. The voltage may become high enough to eliminate the entire depletion region.
An approximation to the current I of a p-n junction is usually written as a function of the diode voltage V_d as

$$I = I_0 \left(\exp\left(\frac{qV_d}{nkT}\right) - 1 \right) \qquad 3.1$$

Where I_0 is the saturation current and n is the diode ideality factor. The ideality factor n incorporates all those unknown effects making the device nonlinear. The diode voltage V_d is the voltage across the space-charge region and excludes any voltage drops across the p and n quasi-neutral regions. K is Boltzmann's constant. T is the temperature of the diode. Here I_0 is temperature dependent. This equation gives a reasonably accurate prediction of the current-voltage relationship of the p-n junction itself, especially due to the temperature variation. The saturation current is given as

$$I_0 = AA^* T^2 \exp\left(\frac{-q\phi_B}{kT}\right) \qquad 3.2$$

Where, A is the area of the diode. A^* is the Richardson constant [1] corrected by the effective mass:

$$A^* = A\left(\frac{m^*_n}{m_e}\right) \qquad 3.3$$

Where m^*_n is the effective mass of the electrons and m_e the mass of the single electron.

If the diode voltage $V_d >> nKT$, equation 3.1 becomes as follow:

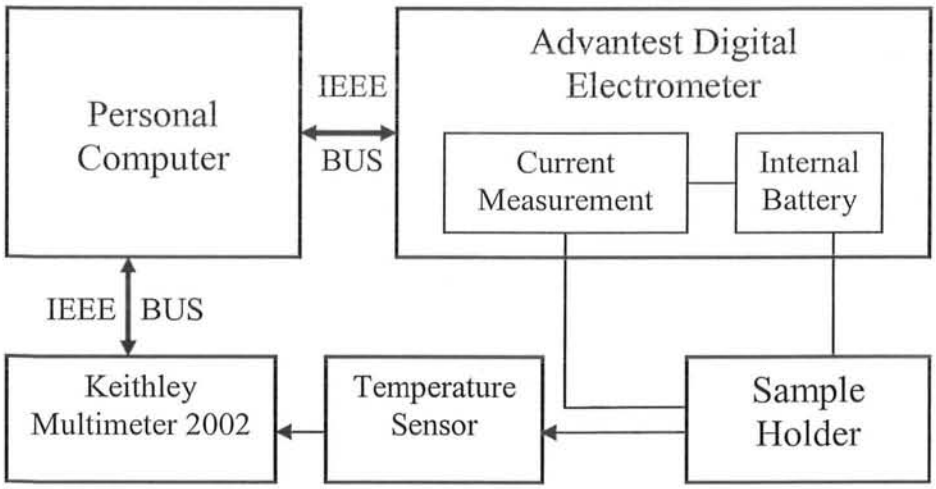
$$I = I_0 \exp\left(\frac{qV_d}{n\,kT}\right) \qquad 3.4$$

The equation 3.4 can be written in linear form by taking the log on both sides of this equation. The linear form of the equation 3.4 is given as:

$$\ln(I) = \ln(I_0) + \left(\frac{qV_d}{nkT}\right) \qquad 3.5$$

This is equation of straight line [2]. We can calculate ideality factor n from the slope of this line. The value of ideality factor n determines which type of current dominates. If the value is $n = \sim 1$, then diffusion current dominates. If the value of n is ~ 2, then recombination current dominates. If $1 < n < 2$ then both currents are present. Where, $\ln(I_0)$ is the intercept of this line. We can also calculate potential barrier height ϕ_B [3] using equation3.2

$$q\phi_B = kT \ln\left(\frac{AA^*T^2}{I_0}\right) \qquad 3.6$$



Block diagram for current-voltage is shown in figure 3.1

3.2 Capacitance –Voltage (C-V) Characteristics

The p-n junction is an interface between two substrates having different doping profiles of silicon. The metallurgical p-n junction is formed by the diffusion of carriers because of their concentration gradient. This metallurgical junction develops two layers of opposite charges at its edges. So this metallurgical junction acts as a capacitor. There are basically two kinds of capacitance associated with this junction. The junction capacitance is due to the dipole of charges in the transition region. It is also called depletion layer or transition region capacitance. As diffusion current increases, voltage lags behind that produces the change in capacitance. This capacitance is called charge storage capacitance. It is often called the diffusion capacitance. The junction capacitance is dominant under reverse bias and the charge storage capacitance is dominant under forward bias.

Capacitance is defined as the differential flow of the charge into plate with respect to the change in applied voltage as follow:

$$C = \left| \frac{dQ}{dV} \right| \qquad 3.7$$

Where Q is charge on each side of the transition region and V is the applied voltage. Since the charge Q on each side of the transition region varies nonlinearly with applied voltage, the width of transition depends on value of applied voltage. Since we are dealing with nonequilibrium case with applied voltage so electrostatic potential barrier changes to (V_0-V). Width of the transition region is given as follow:

$$W = \left[\frac{2\varepsilon\,(V_0 - V)}{q}\left(\frac{N_a + N_d}{N_a N_d}\right)\right]^{1/2} \qquad 3.8$$

Where, N_a and N_d are the concentrations of the acceptor and donor impurities.

It is clear from expression 3.8 that applied voltage V can be either positive or negative for forward or reverse bias. The width of the transition region increases with the decrease in reverse bias and it decreases with increase in forward bias. Since the uncompensated charge Q on each side of the junction varies with the transition region, the value of Q can be written in terms of the doping concentration and transition region width on each side of the junction as follow:

$$|Q| = A\left[2q\varepsilon\,(V_0 - V)\left(\frac{N_a N_d}{N_a + N_d}\right)\right]^{1/2} \qquad 3.9$$

Where A is the area of the sample and ε is permittivity of silicon.

The expression 3.9 shows that the charge Q is nonlinear function of applied voltage. The junction capacitance C_j is calculated from equation 3.7 and after taking derivative of equation 3.8 with respect to potential barrier difference.

$$C_j = \varepsilon A\left[\frac{q}{2\,\varepsilon\,(V_0 - V)}\left(\frac{N_a N_d}{N_a + N_d}\right)\right]^{1/2} \qquad 3.10$$

$$C_j = \frac{\varepsilon A}{W} \qquad 3.11$$

If the junction is asymmetrically doped then the transition region lies primarily into the less heavily doped side, and the capacitance is determined by only one of the doping concentrations. For a $p^+ n$ junction the capacitance is given as follow:

$$C_j = A \left[\frac{\varepsilon q N_d}{2 (V_0 - V)} \right]^{1/2} \quad \text{For } p^+n \qquad 3.12$$

It is possible to measure the concentration of the lightly doped region using equation 3.12

Linearly graded junction diode is that in which the concentration of the ions varies gradually [4].The space charge density $q N_d$ of linearly graded junction varies as:

$$V_j = \frac{q N_d}{12\varepsilon} W^3 \qquad 3.13$$

Junction capacitance of the linearly graded junction can be calculated as

$$C_j = A \left[\frac{\varepsilon^2 q \alpha}{12 V_j} \right]^{1/3} \qquad 3.14$$

Where α is the concentration gradient.

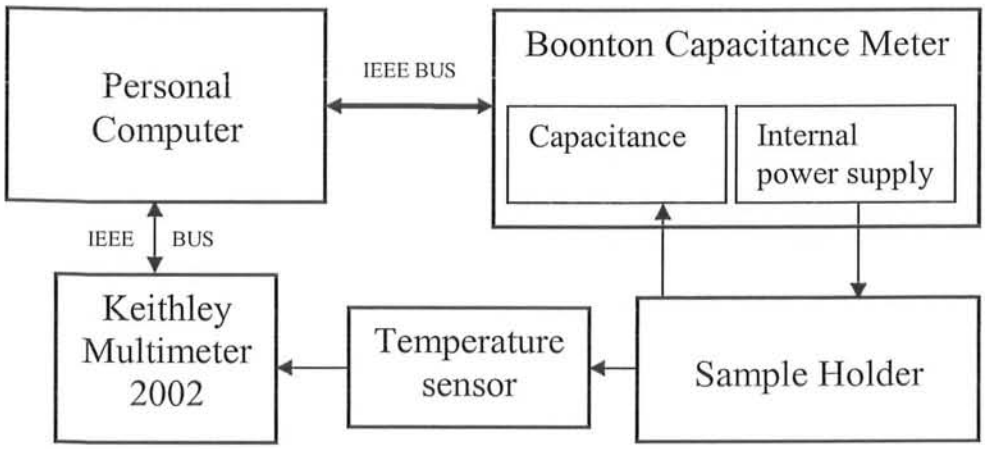


Fig. 3.2 Block diagram for C-V measurements

3.3 Single-Shot Transient Technique.

The equilibrium or steady state of a system can be perturbed by changing the concentration of the carriers. Concentration of carrier can be changed by applied voltage, temperature of the system and light shining. The system is then allowed to relax back. Its relaxation exposes properties of the physical system. Since the temperature has, in many cases, a most pronounced effect on the physical property of the system. So it has to be carefully controlled during the experiment. There are two basic types of relaxation techniques as given below:

- Isothermal relaxation: the system is perturbed at constant temperature and then it is allowed to relax back and change in capacitance is recorded for a long. The transient obtained by such measurements gives the time constant/ constants of the transient and ultimately emission rates are calculated from time constant. This method of recording transient is known as *single shot measurement.*
- Nonisothermal relaxation: the system is perturbed at a sufficiently low temperature to reduce the probability to establish a new equilibrium. Subsequently, the temperature is increased with help of well-controlled heating program. Thus increasing the reaction rates and the relaxation of the system can be monitored as a function of temperature and time [5].

Consider a p^+n junction in equilibrium at a fixed temperature. The charge carrier population in space charge region of p^+n junction can be changed by switching the applied bias from zero to a reverse applied voltage. The deep level are filled for $X > W - \lambda$ and empty for $X < W - \lambda$ as shown in figure 3.3(a) [6]. This perturbation in space charge region will come to an end to attain steady state equilibrium in a finite time. When the deep levels begin to empty, the transient in form of current or capacitance is recorded. The emission rate of the deep levels can be calculated from the time constant of this transient. We can estimate the density of deep levels filled with the carriers in initial state from the magnitude of this transient. Theory of single shot technique is explained as below:

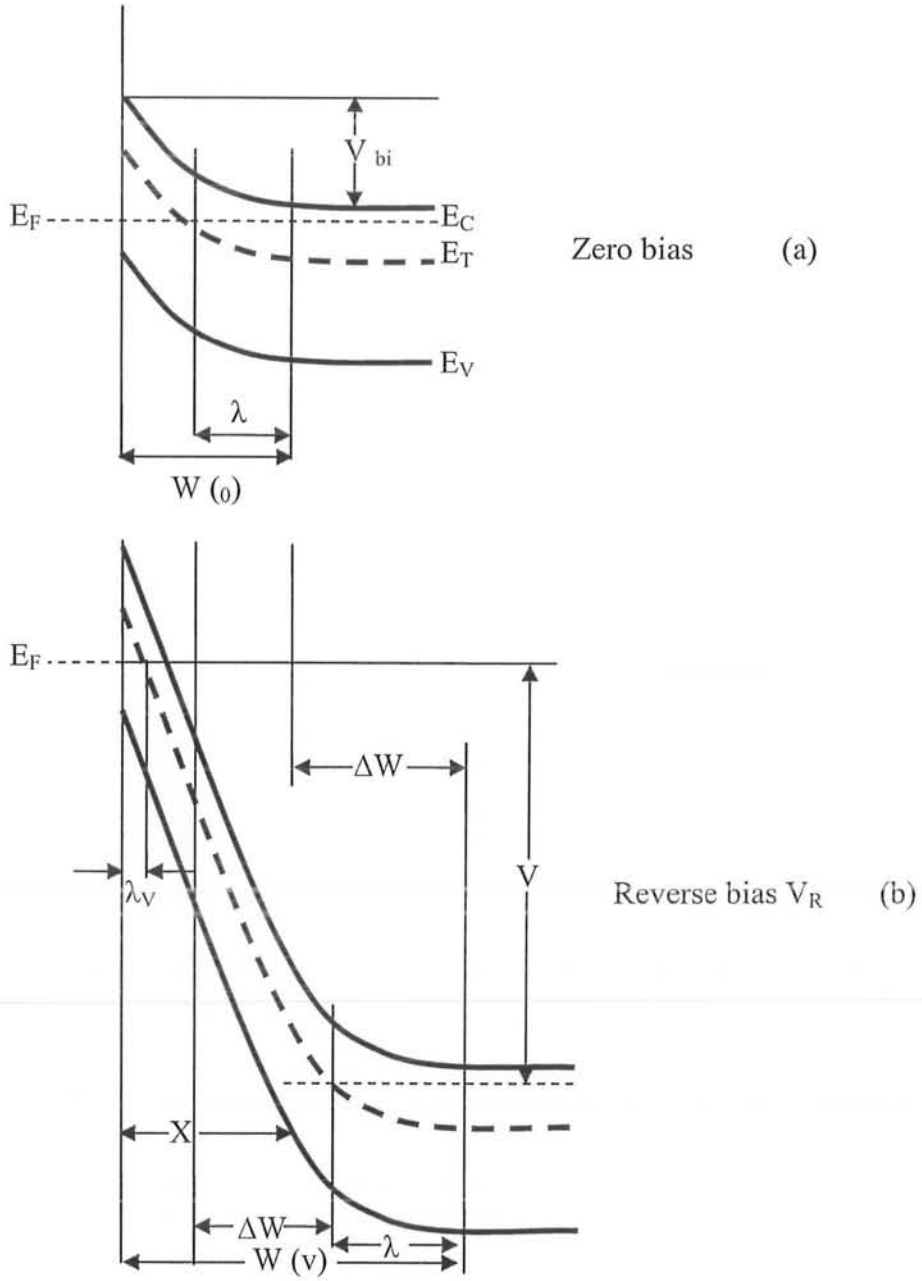


Fig. 3.3 Band bending diagram for p^+n junction [7]

According to Shockley-Read-Hall statistics, the recombination kinetics of the charge carriers introduced into space charge region by perturbation process is governed by the following equation.

$$dn_T/dt = (nc_n + e_p)N_T - (nc_n + pc_p + e_p + e_n)n_T \qquad 3.15$$

In space charge region, electrons 'n'

In space charge region, electrons 'n' and holes 'p' are negligibly small and can be neglected[8,9]. The equation 3.15 can be written as:

$$dn_T/dt = (e_p)N_T - (e_p+e_n)n_T \qquad 3.16$$

The equation 3.16 is first order inhomogeneous. The solutions of this equation under condition $N_T = n_T$ at t=0 are as:

$$n_T = N_T \qquad \text{for } t \leq 0 \qquad 3.17$$

$$n_T = (e_p)N_T/(e_p+e_n)\{1+(e_n/e_p)\exp(-(e_p+e_n)t\} \qquad \text{for } t>0 \qquad 3.18$$

If N_d is positive space charge concentration in the space charge region of the width W, then the voltage change induced by trapped electrons n(x,t) at x in the interval Δx at $0 < x < W$ is given as

$$\Delta V = e/\varepsilon\,[N_d\, W(\Delta W) - n(x,t)\, x(\Delta x)] \qquad 3.19$$

The trap concentration in a space charge region is based on the change in capacitance by the release of the carriers from the trap at constant reverse bias. It is obtained from equation 3.19 by putting $\Delta V = 0$, $C = \varepsilon A/W$ and $\Delta C = \varepsilon A/\Delta W$.

$$\Delta C/C = [n(x,t)/N_d W^2]x\Delta x \qquad 3.20$$

If n(x,t) is only time depended , the electron trapped n(t) are equal to filled traps n_T and $n_T = N_T$ which are uniformly distributed , then equation 3.20 can be written as:

$$\Delta C/C = \int [(e_p)N_T/N_d\, W^2(e_p+e_n)][1+(e_n/e_p)\exp\{-(e_p+e_n)t\}]x(dx) \qquad 3.21$$

After integrating the equation 3.21 while using $W = W_v$ at applied voltage V_R and W_0 at built-in voltage V_{bi} such that $W_v >> W_0$, we get the following equation:

$$\Delta C/C = [(e_p)N_T/2N_d\, W_v^2(e_p+e_n)][1+(e_n/e_p)\exp\{-(e_p+e_n)t\}]\, W_v^2 \qquad 3.22$$

When electrons are majority carriers i.e $e_n >> e_p$ then equation (h) reduces to

$$\Delta C/C = [N_T/2N_d \exp\{-(e_n)t\}] \qquad 3.23$$

$$\Delta C/C = [N_T/2N_d \exp\{-t/\tau\}] \qquad 3.24$$

Where $\tau = 1/e_n$ is the capacitance transient time constant.

$$\Delta C = C\, N_T/2N_d \exp\{-t/\tau\} \qquad 3.25$$

Taking natural log on both sides we get

$$\ell n\, \Delta C = -\, t\,(1/\tau) + \ell n\,(CN_T/2\,N_d) \qquad 3.26$$

This is an equation of a straight line. The slope of the equation gives the emission rate of electrons. For holes the same procedure is used with convenient changes in parameters.

3.4 Deep Level Transient Spectroscopy

`Deep Level Transient Spectroscopy (DLTS) was developed in 1974 by D.V. Lang [10] to investigate energetically "deep" charge trapping levels in semiconductor space charge structures, which may be either pn junctions or Schottky barriers. It utilizes the fact that the reference capacitance of the sample depends on the charge state of deep levels in the space charge region. In total depletion approximation, the reference capacitance of a sample having a homogeneous doping concentration is:

$$C_0 = A\sqrt{\frac{\varepsilon\varepsilon_0 e\,(N_D - N_A)}{2(V_r + V_d)}} \qquad 3.27$$

Here A is the sample area, N_D-N_A is the total net charge density in the space charge layer (SCL), V_r is the reverse bias, $\varepsilon\varepsilon_0$ is the permittivity of the semiconductor material, and e is the electron charge. If the sample is a pn junction, N_D-N_A refers to the lower doped side of the junction. V_d is the built-in diffusion voltage of the space charge structure, which is the crossing point of the extrapolated $1/C^2$ plot vs V_r with the V_r-axis. If A is measured in units of mm^2, N_D-N_A in cm^{-3}, C_0 in pF, and V_r+V_d in V, eq. 3.27 leads to the following relation with adapted units:

$$N_D - N_A\left[cm^{-3}\right] = 1.41*10^{12}\,\frac{C_0[pF]^2\,(V_r + V_d)}{A\left[mm^2\right]^2\,\varepsilon} \qquad 3.28$$

If charged trapping levels are existent in the SCR, their space charge has to be added to N_D-N_A [11]. Assuming a donor-like trap level of concentration N_t in an n-type sample biased under a reverse bias V_r, the capacitance change by recharging these levels is

$$\Delta C = A\sqrt{\frac{\varepsilon\varepsilon_0 e\,(N_D - N_A)}{2(V_r + V_d)}} - A\sqrt{\frac{\varepsilon\varepsilon_0 e\,(N_D - N_A + N_t)}{2(V_r + V_d)}} \cong C_0 \frac{N_t}{2(N_D - N_A)} \qquad 3.29$$

The last identity holds approximatively if $N_t << N_D\text{-}N_A$ holds. Then the trap concentration calculates from the capacitance change ΔC as:

$$N_t = \frac{2\,\Delta C}{C_0}(N_D - N_A) \qquad 3.30$$

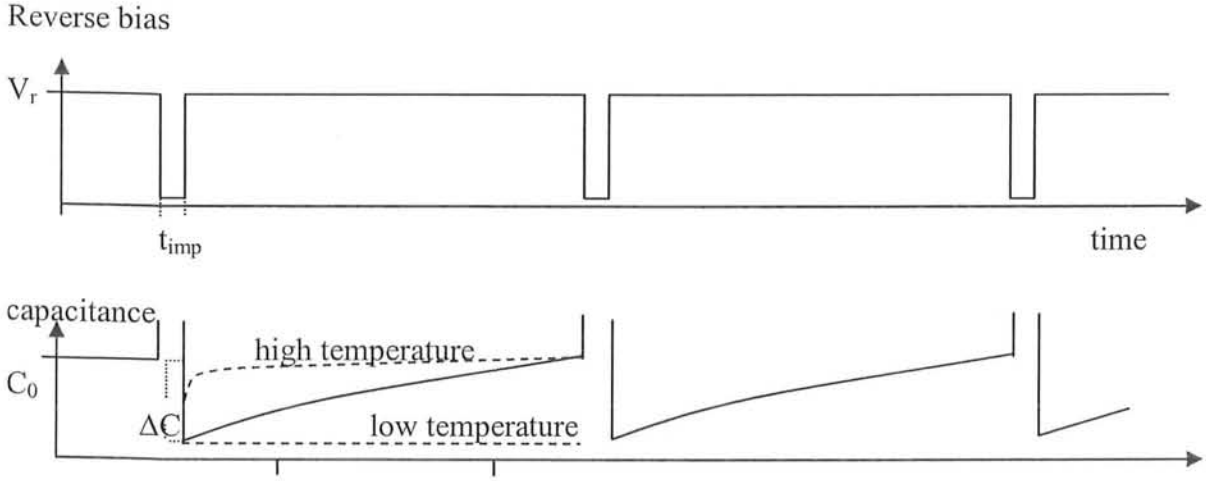


Fig. 3.4

3.5 DLTS Measurement Procedure

The DLTS measurement i.e. the capacitance transient of the sample is measured under the reverse voltage bias V_r when the bias pulses are periodically applied to the sample. This leads to a periodic recharging of the levels in the SCR (Space Charge Region). Its reverse bias V_r is reduced or even reversed for a certain filling pulse width t_p. During these pulses the reference capacitance changes. Immediately after each pulse the reference capacitance changes by ΔC, whereby ΔC is negative for majority carrier traps and positive for minority carrier traps as shown in figure 3.4. If a Schottky diode is used, or if in a pn junction the reverse bias is only reduced by a pulse bias $V_p \leq V_r$, only majority carrier traps are recharged. If during the pulse a pn junction is forward-biased by injection, also minority carriers may be recharged. The degree of trap filling depends on

the filling pulse width t_p and on the capture coefficient of the traps $c_{n;p}$, which is often formally expressed as the product of the thermal velocity times the capture cross section of the trap for the corresponding carrier type. For the filling of traps in space charge region (SCR), the pulse width t_p of the pulse should be large enough with the pulse period t_w. Hence all deep levels in the SCR will be filled by the pulse. For sufficiently small pulses only some part of all levels are filled, hence the signal gets smaller. The pulse width t_p, for which the signal height has reduced to $1/e = 0.367$ of its maximum value, allows one to measure the capture coefficient c_n for electrons or c_p for holes:

$$C_{n;p}=(n;p)/\ t_p \qquad 3.31$$

Here n and p are the free carrier concentrations of electrons and holes, respectively, during the capture process. Equations 3.30 and 3.31 only hold if ΔV is large compared to V_d and close to V_r. For $\Delta V < V_r$ the trap concentration calculated for saturation pulses for homogeneous trap distributionis is as follow:

$$N_t = \frac{2\,\Delta C\,V_r}{C_0\,\Delta V}(N_D - N_A) \qquad 3.32$$

Hence, for homogeneous trap distribution the DLTS peak height ΔC is expected to be proportional to the filling pulse height ΔV. Note that the equilibrium degree of trap filling in the SCR under reverse bias is zero, hence the levels are ionized. If after a filling pulse traps are filled and the reverse bias is re-established, the system is in thermal non-equilibrium and relaxes into equilibrium by thermally emitting the trapped charges into the corresponding bands, where they are swept away by the electric field. For isolated point defects this relaxation is exponential in time, but for extended defects like dislocations, precipitates, and interface layers the emission transient i.e. just as the trap filling process, may be non-exponential. Therefore all these relations strictly only hold for point defects. This relaxation is connected with a capacitance transient, which is converted into a measurable transient signal by a capacitance-meter [12]. The time constant τ_e of the thermal emission is governed by the thermal emission rate $e_{n;p}$, which depends on the trap energy E_t and on the temperature T:

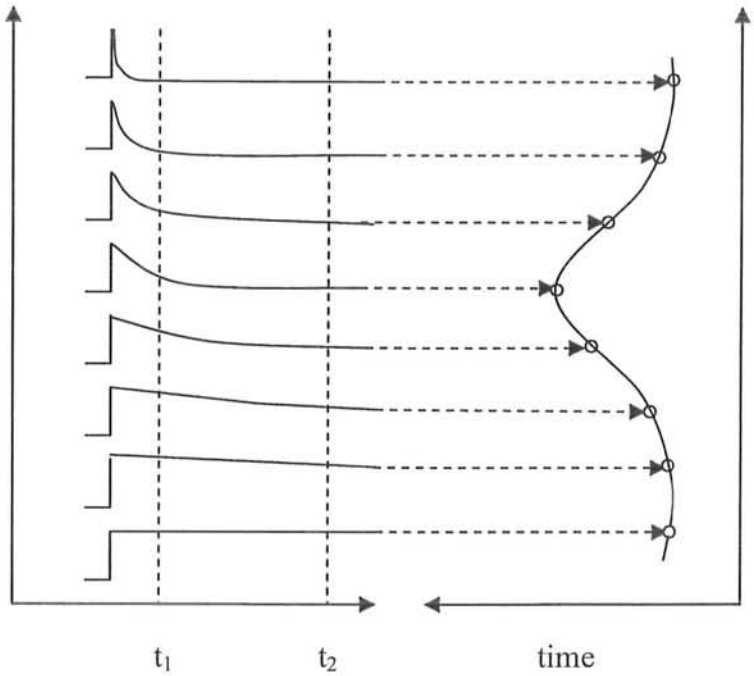
$$e_{n;p} = \frac{1}{\tau_e} = \frac{N_{c;v}\, c_{n;p}}{g} \exp\left(\frac{-E_t}{kT}\right) \qquad 3.33$$

Here $N_{c;v}$ is the effective density of states in the conduction band for electron emission or the valence band for hole emission, respectively, g is the degeneracy factor of the level, usually assumed to be unity, and kT is the thermal energy. Hence, the thermal emission rate $e_{n;p}$ is the inverse of the emission time constant τ_e. The exponential dependence of the emission rate on 1/T that is called the Arrhenius plot, with the thermal energy E_t determining its slope and the capture coefficient $c_{n;p}$ determining its prefactor, is the signature of each trap, which is used for their identification.

In DLTS filling pulses are applied periodically to the sample, leading to periodical capacitance transients as shown in figure 3.4. The basic idea of DLTS is to convert the capacitance transients into the DLTS-signal by "correlating" them on-line. The simplest kind of DLTS correlation is the 2-point correlation, where the capacitance is measured at two times t_1 and t_2 after the end of each filling pulse, and the difference between these two values is displayed:

$$\text{Output signal} = a[C(t_2)-C(t_1)] \qquad 3.34$$

Hence, the DLTS signal is scaled in units of capacitance (usually pF) [13,14]. Other kinds of correlation are providing an especially good signal-to-noise ratio (exponential correlation) or a better energy resolution (high resolution correlation) than 2-point correlation. Usually the DLTS measurement starts at low temperature, the temperature is slowly ramped up, and the DLTS signal is recorded. During the T-ramp the relaxation time constants of all levels in the sample are gradually increasing from very large values to very low ones according to eq. 3.33. As long as T is too low for significant thermal emission until t_2, the difference is zero (eq 3.34). It is shown in "low temperature" trace in figure 3.4. If T is so high that the relaxation is already over at t_1, the difference is also zero and it is shown in "high temperature" trace in figure 3.4 Only if the emission time constant or the emission rate, respectively, of one level falls into the so-called "rate window" given by the selection of t_1 and t_2, a DLTS peak appears [15,16]. For 2-point correlation we obtain the following condition for the DLTS peak to appear:



Emission rate at Peak Temperature $e_{max} = \frac{\ell n(t_1/t_2)}{t_1 - t_2}$

Fig. 3.5 (b)

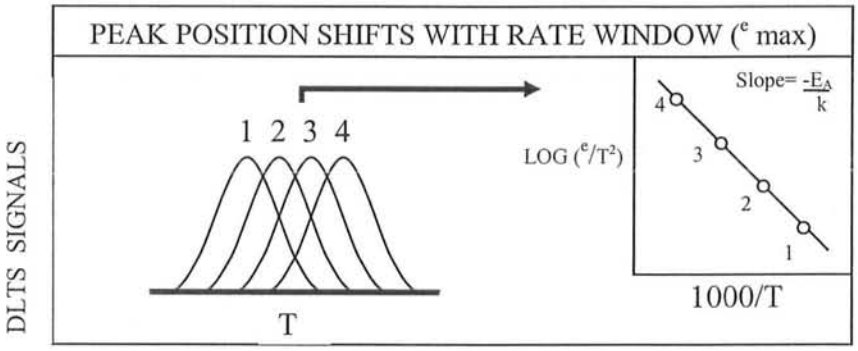


Fig. 3.5 (c)

3.6 Deep Level Defects Characteristics

Deep level defects present in space charge region are characterized by different parameters. These parameters are tools to know all about the nature of these defects. Detailed knowledge is necessary about these parameters. Without these we are not able to have conformed information about their binding energy, depth profile, and nature of the defects. Following are the parameters of deep level defects which are usually studied using DLTS technique.

- Thermal Emission Rate
- Thermal Activation Energy
- Deep Level Concentration
- Capture Cross-sections

3.7 Thermal Emission Rate

When p^+n junction is biased by applying sufficiently high reverse bias but smaller than the breakdown voltage followed by repeated pulses from this reverse bias to close-to-zero volt , transient due to emission of the charge carriers recorded by DLTS. The temperature of the sample is continuously changed. Emission and capture processes are present there [19, 20]. The net rate of electron emission is given by

$$dn_T/dt = c_n p_T n - e_n n_T \qquad 3.36$$

When junction is perturbed by reverse bias, the number of filled and unfilled traps will change due to this perturbation. The transition of the effected levels will decay to steady state at time $t = \infty$ i.e

$$e_n n_T(\infty) = n c_n \quad p_T(\infty) \qquad 3.37$$

In steady state condition, the change in filled and unfilled traps is equal i.e $n_T = - p_T$, so the net rate of change of trapped electrons can be written as

$$dn_T/dt = c_n p_T n - e_n n_T = (c_n n + e_n)\Delta p_T$$

Or

$$dn_T/dt = (c_n n + e_n)\Delta n_T \qquad 3.38$$

The quantity $(c_n n + e_n)$ remains constant during the time t, the solution of the equation 3.38 is given as

$$n_T(t) = n_{T(0)} \exp [-t (e_n n\, c_n)] \quad 3.39$$

Putting the value of c_n from equation 3.36 into equation 3.39 we get

$$\Delta n_T = n_{T(0)} \exp [-t\, e_n \{ p_T(\infty) + n_T(\infty)\}/p_T(\infty)] \quad 3.40$$

The occupancy of the electron by the trap is define as

$$f = n_T/ (n_T+p_T) \quad 3.41$$

From equation 3.40 and equation 3.41 we get

$$f(t) - f(\infty) = (f_0 - f_\infty) \exp \{(- te_n)/ (1 - f_\infty) \} \quad 3.42$$

If the final state is empty in that case $f_\infty = 0$ then equation 3.42 becomes as

$$f(t) = f(_0) \exp (-e_n t) \quad 3.43$$

Taking natural log on both sides, the equation becomes as

$$e_n = - 1/t\, \ell n \{ f(t)/ f(_0)\} \quad 3.44$$

It is clear from equation 3.44 that the emission rate of the electrons is reciprocal to the time constant of the transient.

Emission process is shown in figure 3.6

3.8 Thermal Activation Energy.

According to Shockley- Read-Hall theory, the emission rate of the carriers can be related to the capture cross-section as given below,

$$e_n = \sigma_n \langle V_n \rangle N_c \exp \{ - (E_c - E_T)/ (kT)\} \quad 3.45$$

Similarly emission rate for hole traps is given below as

$$e_p = \sigma_p \langle V_p \rangle N_v \exp \{ - (E_T - Ev)/ (kT)\} \quad 3.46$$

We can proceed from above equations to calculate the activation energy of electrons and holes respectively. But we will consider only the case of electron trap. These parameters depend on the temperature.

The $V_{n,p}$ has $T^{1/2}$ because $V^2 = \{ (3kT)/(m)\}$

Similarly $N_{c,v}$ has $T^{3/2}$ temperature dependence. The equation 3.45 can be written in term of temperature as follow;

$$e_n = AT^{1/2} T^{3/2} \sigma \exp \{(\Delta E)/(kT)\}$$

$$e_n = AT^{2} \sigma \exp \{(\Delta E)/(kT)\} \quad 3.47$$

Where, A is constant.

$$\Delta E = E_c - E_T \quad \text{for electrons emission} \quad 3.48$$

$$\Delta E = E_v + E_T \quad \text{for hole emission.} \quad 3.49$$

Taking natural log on both sides of the equation 3.47 we get a equation of straight line [21].

$$\log (e_n / T^2) = \log (A\sigma_n) - \Delta E/kT \quad 3.50$$

The slope of this line gives the activation energy of level.

3.9 Deep Level Concentration

This is another parameter by which the number of emitted or trapped carriers from the deep level at temperature is calculated. When a p^+n junction is reversed bias, the electrons are emitted from those levels which were filled before the application of reverse bias. Emission of these electrons from space charge region changes the capacitance of the junction. This process will continue for a finite time until all the levels above the Fermi level become empty. When high reverse voltage but less than breakdown voltage is applied for such a finite long time to the junction the change in capacitance will tend to maximum. The finite time and maximum change in capacitance can be denoted as $t_{(\infty)}$ and $\Delta C_{(\infty)}$ respectively. Maximum change in capacitance can be written as

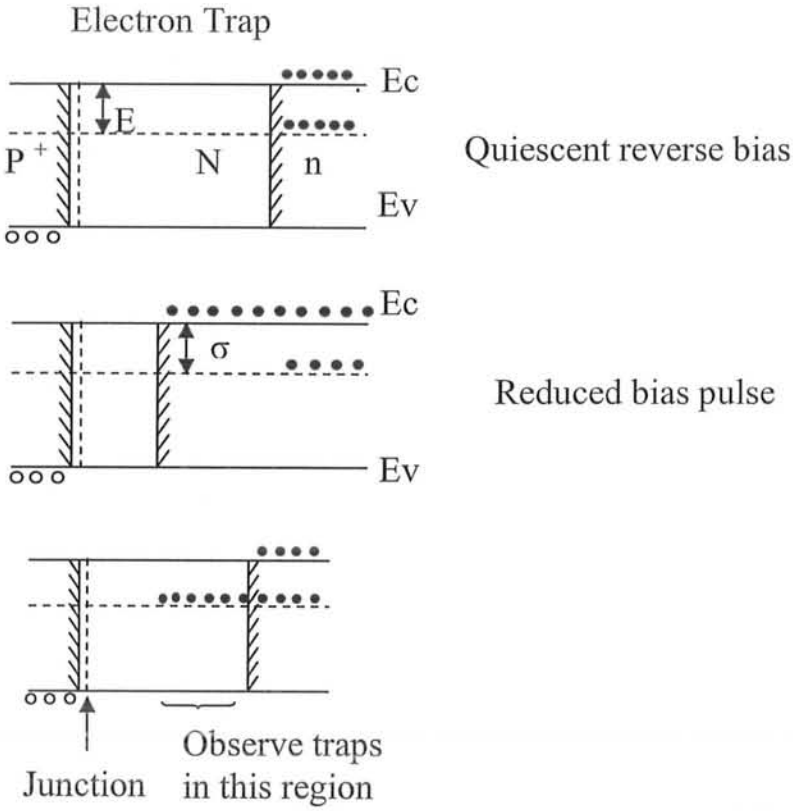
$$C_{(\infty)} - C_{(0)} = \Delta C_{(\infty)} \quad 3.51$$

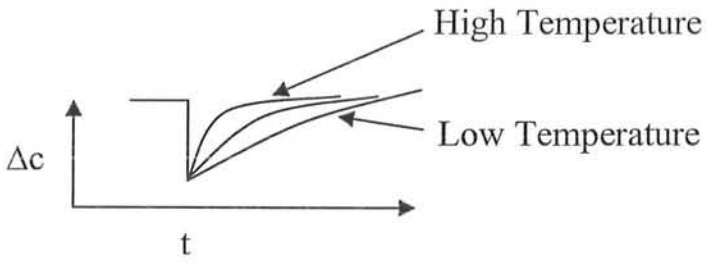
Change in capacitance per unit capacitance is derived in single shot technique which is given as follow:

$$\Delta C/C = [N_T/2N_d \exp\{-t/\tau\}] \quad 3.52$$

Where $\tau = 1/e_n$ is the capacitance transient time constant.

When $t \rightarrow \infty$ then $e_n = 0$ and $\Delta C = \Delta C_{max}$ Applying these conditions to equation 3.52





Capacitance Transient

Fig. 3.6

We get as

$$\Delta C_{max}/C = N_T / (2\ N_d) \qquad 3.53$$

$$N_T = (\ \Delta C_{max}/C\ )\ 2N_d \qquad 3.54$$

Where N_T is the deep level concentration and N_d is the shallow level concentration.

3.10 Capture Cross-Section

Consider a p^+n junction which is biased by a filling pulse. This filling pulse will fill the carriers' traps. If filling time of the pulse is increased then number of the carriers trapped will increase. DLTS scan is taken; the peak of the spectrum corresponds to the emission rate of the carriers. The peak height varies with varying pulse width for a fixed rate window in emission spectrum. The rate of change of filling trap concentration n_T during the zero bias filling pulse is given as

$$dn_T/dt = S_n\ (N_T - n_T) \qquad 3.55$$

The solution of the equation 3.55 is given by

$$n_T = N_T[\ 1- \exp\ (-S_n\ t)] \qquad 3.56$$

Where $S_n = nc_n = \sigma_n\ n < V\ th_n >$

When steady state reverse bias is restored after the capture time t_c the filled trap concentration after time t in the upper half of the band gap cab be written as

$$n_T(t_c,t) = N_T[\ 1- \exp\ (-S_n\ t_c)]\ \exp\ (-t/\tau_n) \qquad 3.57$$

Where $e_n = 1/\ \tau_n$ and t is the time measured after the restoration of steady reverse bias. Change in capacitance depends on the change in occupancy of the traps. Change in capacitance of the junction after t_c can be related to maximum change in capacitance after infinite capturing time is given as

$$\Delta C\ (t_c) = \Delta C\ (\infty)\ [1 - \exp\ (-S_n\ t_c)]$$

$$[1- \Delta C\ (t_c)/\ \Delta C\ (\infty)] = \exp\ (-S_n\ t_c) \qquad 3.58$$

Taking natural log on both sides of the equation 3.58 gives the equation of straight line. The slope of this line gives the capture rate S_n.

The capture cross-section can be calculated by putting respective capture rates in following equations

$$S_n = \sigma_n \, n\langle V_{thn} \rangle \qquad \text{For electrons} \qquad 3.59$$

$$S_p = \sigma_p \, p\langle V_{thp} \rangle \qquad \text{For holes} \qquad 3.60$$

Where V_{th} is thermal velocity of the carriers.

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CHAPTER

4

Development of Digital Computerized DLTS System

4.1 Introduction

A computerized system for deep level characterization in semiconductor has been setup in our laboratory, with the possibility of enhancing both hardware and software. It is based on the well known Deep Level Transient Spectroscopy (DLTS) technique [1]. This system has been setup at much lower cost than commercial systems. A digital approach to the signal processing in deep-level transient spectroscopy (DLTS) systems is introduced. An improved digital averaging scheme for DLTS signal recovery from noise and transient data storage is proposed. Digital averaging techniques can improve the DLTS digital signal processing. Digital averaging techniques are pseudo-logarithmic time averaging and continuous time averaging. Continuous time averaging is well suited for improving overall signal-to-noise ratio (SNR). It is suitable for continuous display and processing of data, and it is more efficient in using the computer resources. This digital computerized DLTS system is based on continuous time averaging technique. The theory of continuous time averaging technique is explained as:

4.2 Theory of Continuous Time Averaging Technique

The pseudo-logarithmic averaging is a very efficient technique for reducing the number of data points and for SNR improvement at relatively high frequencies and large delay times. But it is not suitable at low frequency noise and to improve the SNR at the beginning of the transient. However, the continuous time averaging [2] is a very convenient technique for above mentioned purposes. In addition, it has the advantage of allowing continuous transient display after each pulse and the size of the allocated memory buffer is independent of the number of averaged transients. The continuous time averaging mode is similar to the running average formed by a low-pass filter. Low-pass filter averages the data points consecutively in time so that low-pass filters can not be applied to the multiple times averaging. Multiple time averaging processes the whole set of transient data points in parallel, i.e. each data point is averaged with corresponding data points from the other transients which are at the same delay from the start of the transient. In this way the data points to be averaged are separated by one or more pulse periods and are not consecutive in time

Since the introduction of deep-level transient spectroscopy (DLTS) in 1974 by Lang [3], the method has been refined many times with new techniques for improving the sensitivity and accuracy, and for simplifying the measurement and data analysis procedures. At present, DLTS is comprised of a large group of different measurement techniques applied to a variety of test devices and materials. It is considered to be among the most accurate and reliable tools for investigating the properties of electrically active point defects in semiconductors [4].

Working principle of DLTS is based on some common features of all DLTS technique as: First, it is the time domain measurement of the emission of the charges trapped in electrically active centers. Second, this process is thermally activated and is based on Shockley-Read-Hall theory. Third, there is periodic alternation between filling of the traps with charge and emission of the trapped charge. This last feature is used for synchronized measurement and integration. This is the basic method used for signal recovery from noise in electronic instrumentation [5]. The DLTS experiment can be

consisted of several steps. The first step is to detect the change of the trap occupancy with electrons as a measurable change in capacitance of the space charge region. The next steps are synchronous detection and averaging of this signal in order to improve the signal-to-noise ratio (SNR). There are two main approaches i.e. the use of analog or digital signal processing methods.

4.3 Analog Methods

The noisy transient signal can be measured and integrated over many pulses using analog instruments such as a boxcar averager [6], a lock-in amplifier [7], or an exponential correlator [8]. In the classical setup, two boxcar channels are used to measure the signal at two different times in the transient, and these times define a time constant window of the instrumentation [9]. The averaging is performed by the boxcar channels and the difference versus the sample temperature is recorded, giving a DLTS spectrum. When the emission time constant of a deep level coincides with that of the instrumentation while scanning the temperature of the sample, the output signal indicates this coincidence with a peak in the spectrum. To apply the Arrhenius relationship to determine the energy level and the capture cross section of a trap, several temperature scans are needed using different settings of the time constant window of the instrumentation. Similarly, it is necessary to change the pulse frequency when using a lock-in amplifier, or the reference time constant when an exponential correlator is used, and to repeat the temperature scan in order to obtain enough data for the Arrhenius plot technique. In all these cases, the averaging technique simultaneously achieves two different goals - increasing the SNR and analyzing the transient parameters.

4.3.1 Advantages of Analog Methods

- Analog methods are simple to implement.
- Fast method.
- They produce an analog signal in real time.
- It is easy to plot this signal versus the temperature for spectrum-like curves

4.3.2 Disadvantages of Analog Methods

- One has to perform many temperature scans.
- It can not resolve closely spaced energy levels of defects
- It is difficult to do analysis of non-exponential transient

4.4 Digital Methods

The digital methods record the whole transient as a set of data points. The noisy signal is first digitized and then processed using various digital techniques [10]. The transient parameter analysis can take place during the experiment, or data can be stored for later analysis. The transient can be analyzed using Spectral Analysis DLTS (SADLTS) [11-12], Fourier Transform Analysis [13-15], nonlinear least square fitting [16], the modulation function method [17], the method of moments [18-19], the correlation method of linear predictive modeling [20], or other digital methods described [21]. Since the whole transient is recorded, it is necessary to perform just one experimental temperature scan, which greatly reduces the time needed to perform the experiment.

4.4.1 Advantages of Digital Methods

- One has to perform just one temperature scan.
- It can resolve closely spaced energy levels of defects
- It has extensive possibilities for data analysis.

4.4.2 Disadvantages of Digital Methods

- It is not fast method as compare to analog method.
- Digital methods are not easy to implement
- The total numbers of stored data points are very large compare to analog methods.

- The greatest disadvantage of the digital method that is concerned with resolution of ADC, capacity of the memory buffer, and frequency of the testing pulse is explained as:

In digital method, the whole set of data points are recorded for the transient. Collection of data points depends on the resolution of 12-bit or 16-bit analog-to-digital converters (ADC) and frequency of the testing pulse. The 12-bit ADC has conversion time below 10μs that is interfaced between analog output of capacitance meter and a PC. If 12-bit ADC in operated at frequency of 100 KHz, with the time interval between two data points is 10μs for one degree interval over a temperature range of 50-350 K, then there are 131,072 sampling points which are stored into a 256 kilobyte buffer. From this large set of data, only 768 data points are selected and used, while the remaining 130,304 points are discarded. Second, after averaging, the buffer is cleared for processing of the new transient, and the old information is lost, thus making it more difficult to maintain high SNR. Third and most important, there is a substantial decrease in the SNR, especially in the tail of long transients, where the data point intervals are in the millisecond range, because the data points are selected from just 10 μs long sampling intervals. In addition, recording of 768 data points for each degree in the 50 - 350 K range still requires almost 0.5 Mb disk space and Direct Memory Access (DMA) transfer into memory blocks larger than 64 Kbytes is complicated, since it requires continuous initialization of the DMA controller for crossing the memory page boundary [22].

This digital computerized DLTS can be divided into two parts:

(a) DLTS Hardware (b) DLTS Software.

4.5 Hardware of Digital Computerized DLTS System

This digital computerized DLTS has following hardware:

- Capacitance Meter.
- Pulse Generator.
- Digital Multimeter

- Cryostat
- Oscilloscope
- PC
- Interfacing unit
- Coupling circuit

4.5.1 Boonton Capacitance Meter

Boonton Capacitance Meter, Model 7200 is used to record the capacitance transients of the sample under the different sets of parameters in DLTS measurements. This versatile capacitance meter can measure the capacitance transients in digital and analog form. The Model 7200 is a microprocessor-based, fully automatic, and can measure upto 1MHz capacitance and loss measurements. Its capacitance range is 0 to 2000 pF, and its conductance range is 0 to 2000 μS. The Model 7200 utilizes a 1 MHz test signal with programmable levels of 15, 30, 50, or 100 mV. It accepts, measure, display internal and external DC bias voltages over a range of ±100 Volts and ±200 volts respectively. Bias voltages of either polarity can be applied to the Hi terminals. This bias capability with fast responding C, G, and V outputs makes the instrument ideal for C-V or G-V plots, as well as DLTS studies. The Model 7200 uses a microprocessor with a fixed internal program for the automatic control of all measurements, computation, and display function. The use of microprocessor facilitates interfacing with advance technology extended (ATE) system. The Model 7200 is equipped with a full-function IEEE-488.2 bus interface. Functionality of the C-meter can be made versatile through programming using IEEE-488.2 bus interface Mnemonics. All front panel control function can be programmed, exception of the POWER ON and PLOT keys.

Response time of capacitance meter is 20 readings per second. So it takes 50 milliseconds for one reading. This is not a good response time because 2-points rate window can not be applied for frequency more than 10Hz. Bridge circuit of capacitance meter can not record capacitance more than this response. Efficiency of the capacitance can be improved if this bridge is bypassed and ADC of higher resolution is used.

Efficiency of the capacitance can also be improved using analog output through data acquisition card of better resolution.

4.5.2 Pulse Generator

In DLTS measurements, pulses of different parameters have to apply to the sample at different temperatures. Agilent Model 81110A pulse/ pattern generator is used for this purpose. Model 81110A Pulse and Pattern Generator generates all standard pulses, digital patterns and multi-level waveforms needed to test current logic technologies such as TTL, CMOS, ECL, PECL, LVDS, GTL and digital design up to 330 MHz. The Model 8111A provides a reliable and wide range of signals with selected set of parameters for many applications. The Model 81110A is fully automatic and IEEE-488.2 bus interface. Generation of signals, adjustment of parameters, and application of these signals is programmable and controllable by software through IEEE-488.2 bus interface. This leaves the user free to concentrate on the measurement task and testing of the device under test (DUT). The Model 81110A has a feature of graphic display showing all pulse parameters at a glance. The Model 81110A has internally connected two modules for outputs in normal and compliment form. This pulse generator has memory card which can be programmed and saved. These saved programs can be loaded at any time and run through software or manually. Capacitance meter and pulse generator is interfaced with computer through GPIB Card and synchronized through the software.

4.5.3 Digital Multimeter

Electric and thermal characteristics of the semiconductor materials are temperature depended. These characteristics are measured at different temperatures. The Model 2002 Multimeter of Keithley is used to measure the temperature through thermocouple. This model can be configured from front panel or through the IEEE-488.2 bus interface. This model can store and recall the readings and setup data from the front panel or over the IEEE-488.2 bus. The buffer can be programmed to store up to 850 readings at 4.5 digits, or up to 250 time-stamped readings at 6.5 digits. The Model 2002 can be configured with memory options that extend the storage capacity up to 30,000

readings and ten setups. This model is capable of acquiring 2000 readings / second at 4.5 digits of resolution and 215 readings / second at 6.5 digits. This model has internal scanner card. This card has 10-channels for scanning different analog parameters at the same time. Eight channels are of 2-pole relay switching and two channels of 2-pole solid-state switching. All channels can be configured for 4-poles.

4.5.4 Cryostat

A bath type cryostat has been designed in our laboratory and was made our departmental workshop. This cryostat consisted of two parts. One is for cooling and other is for mounting sample and evacuating the chamber. The chamber can be evacuated through brass pipe. Pins of TO-5 header are connected to BNCs by means of copper wires passing through the brass pipe. A cooling part consists of a liquid nitrogen dewar for external cooling and a mini built in liquid nitrogen reservoir. Liquid nitrogen can circulate in the sample holder through pipes connected to a liquid nitrogen source. Cryostat can be heated using heating coil connected to the controlled power supply. Temperature can also be changed by moving up and down the sample holder within the dewar. Hot end of the copper-constant thermocouple is place very near to sample under studies and the cold end/ reference is maintained at 77 K by dipping it constantly into liquid nitrogen. Output (emf) of the thermocouple is connected to one of the channels of the scanning card of the Keithley digital Multimeter Model 2002. This meter is connected PC through IEEE Bus. All parts of the cryostat are shown in the figure 4.1

4.5.5 Interfacing Units

All devices of this digital computerized DLTS are interfaced with computer through GPIB cards and IEEE-488.2 data cables. These cables are also called Centronics adaptors. These devices are configured at different addresses for proper communication among them. Block diagram of DLTS is shown in the figure 4.2

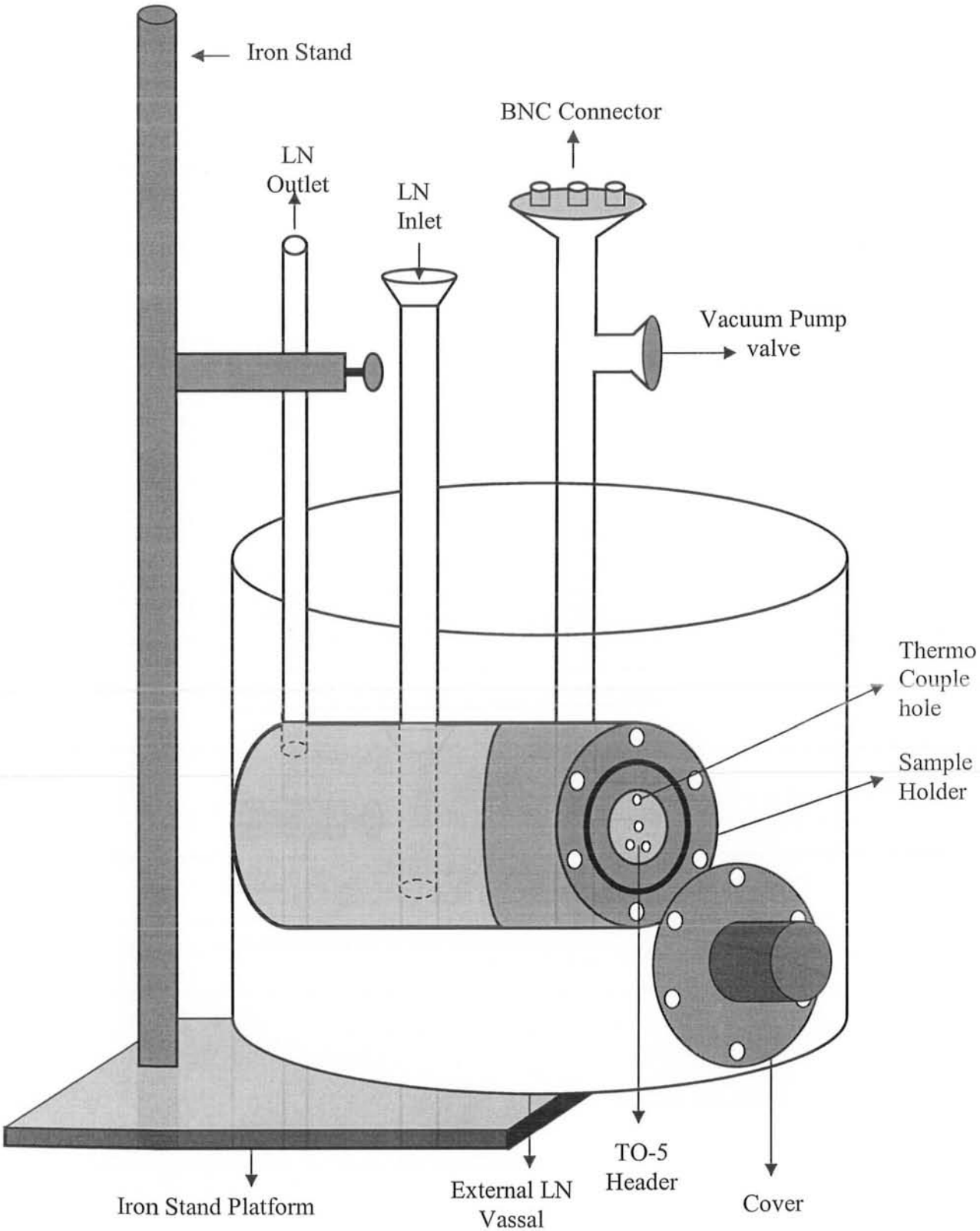

Fig. 4.1 Diagram of Cryostat

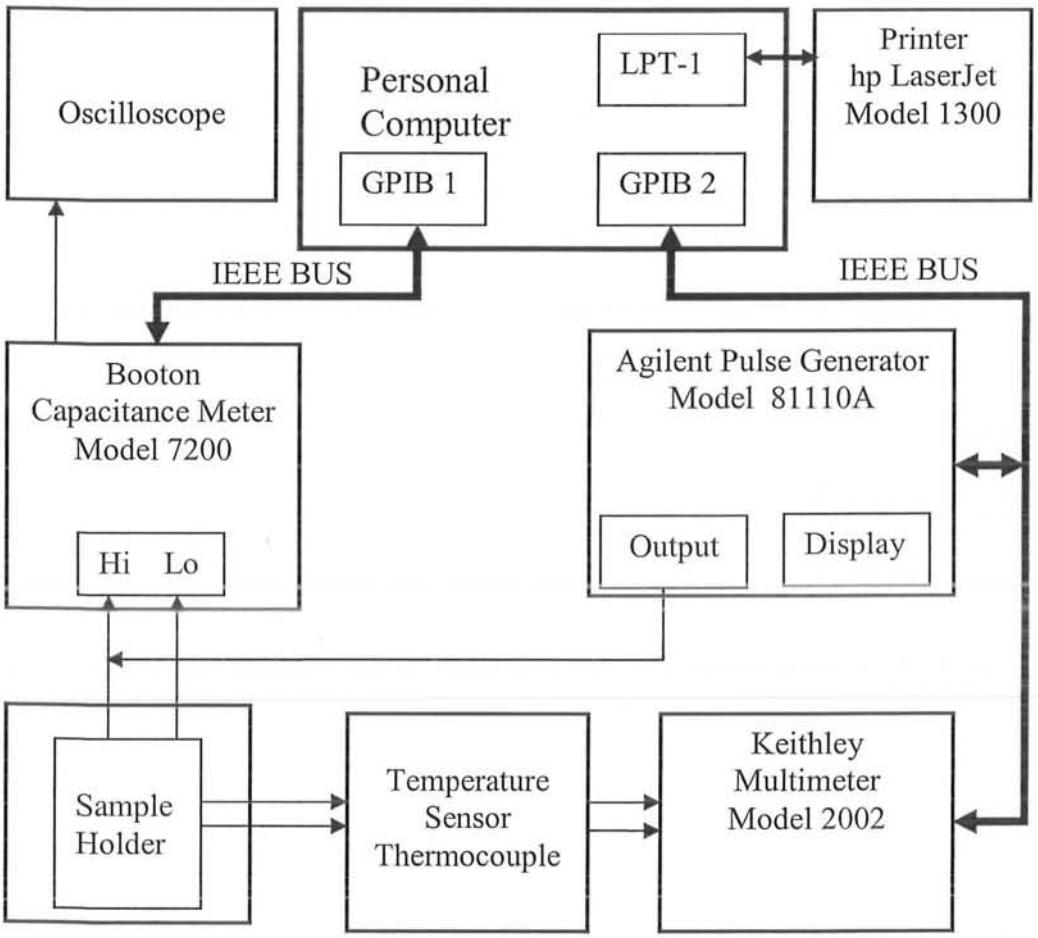

Fig. 4.2 Block diagram of Digital Computerized DLTS

4.5.6 Coupling Circuit

Filling pulses are applied to the diode for DLTS measurements. Short pulses can not be applied directly to the Boonton 7200 capacitance bridge. This capacitance bridge can not detect these short pulses for filling the traps of the diode. Boonton Electronics provided coupling circuit for coupling short pulses onto diode for their Boonton 7200 capacitance bridge. Original coupling circuit was modified to meet the requirement of the DLTS measurements. With this pulse coupling circuit it is possible to use filling pulses well below 0.5 ms in DLTS measurement. The circuit is developed on printed circuit board (PCB). This circuit is attached directly with the BNC connectors onto the capacitance bridge. The shortest pulses that can be applied onto diode using this circuit are about 100ns. The diode is connected to the capacitance bridge by the two "TEST" outputs. A positive bias can be applied to the diode from the internal voltage source as well as from external source in such away, that it is in reverse direction. However, the pulse coupling circuit only works with positive applied voltage. The diode is shortened when a TTL (Transistor-Transistor Logic) pulse of +5V is applied at input. Ripples can be removed from voltage pulse signal on diode by adjusting variable resistor. RC time constant of the circuit has to adjust which is limiting factor for short pulses. Coupling circuit is shown in the figure 4.3

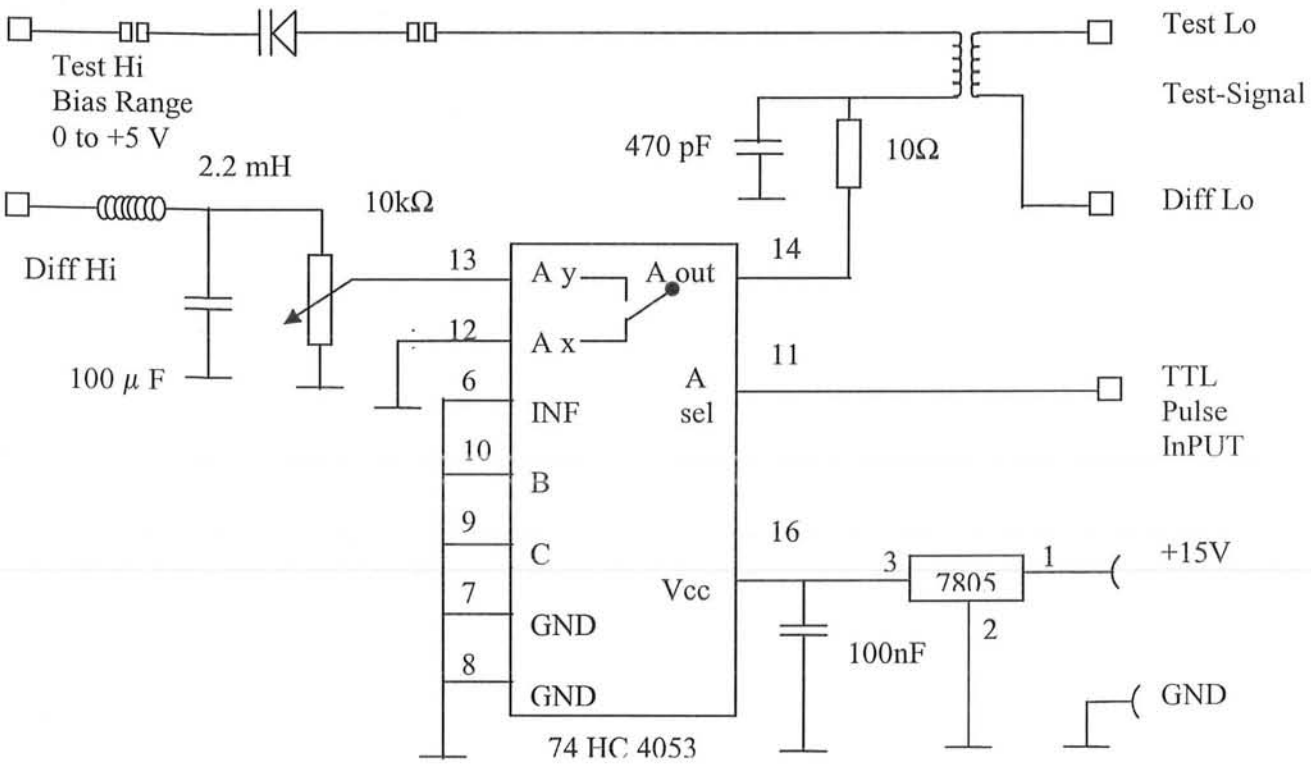

Fig. 4.3 coupling Circuit for Fast Pulsing

4.6 Software of Digital Computerized DLTS System

4.6.1 Introduction

Digital computerized DLTS system is consisted of a capacitance meter, pulse pattern generator, Multimeter, and temperature controller. These devices are interfaced with computer through two GPIB Cards. Software has been written in Microsoft Visual C++ to communicate with these devices. The NI (National instrument) Standard Protocol is used for initialization and termination of device for Talk and Listen operations through computer. Devices are configured at different addresses for proper communication. Capacitance meter, pulse generator, and Multimeter are interfaced with computer through IEEE488.2 output connectors or centronics cables of these devices. All these devices are internally programmed on same set of NI-488.2 commands. The NI-488.2 API has two set of commands or calls to meet application needs. Both of these sets, the traditional commands and the multi-devices commands, are compatible with computer hardware and operating system. We can do programming with little or no source code modification for other platforms. For simple applications, the traditional NI-488.2 commands are sufficient. The multi-devices NI-488.2 commands are used for complex configuration with one or more interfaces. For any set of commands, the bus management operation necessary for device communication are performed automatically.

4.6.2 Communicating With a Single GPIB Device.

If system has only one device attached to each interface, the traditional NI-488.2 commands are sufficient for programming needs. A single device application has three phases:

- Initialization: To get a handle use ibdev and to clear the device use ibclr.
- Device Communication: To communicate with device use these calls: ibwrt, ibrd, ibtrg, ibrsp, and ibwait,
- Cleanup: To put the handle offline use ibonl.

4.6.3 Communicating With Multiple GPIB Devices

The multi-device NI-488.2 commands are used for a system which is interfaced with multi-GPIB Cards and multi-devices configurations. These commands perform the following operations with single command:

- Find the listeners on the bus using Find Lstn.
- Find a device requesting service using Find RQS
- Determine the state of the SRQ line, or wait for SRQ to be asserted using Test SRQ or Wait SRQ.
- Address multiple devices to receive a command using Send List.

4.6.4 Global Status Variables

Each NI-488.2 Application Programming Interface (API) call updates four global variables to reflect the status of the device or interface. These global status variables are the status word (ibsta) the error variable (iberr), the count and control variables (ibcnt and ibcntl). These variables contain useful information about the performance of application. Program checks these variables after each NI-488.2 call and makes decision for further processing.

This software is written in C++ for initialization and uninitialization of device from online. The program is coded in term of the global status variables, traditional and multi-devices commands. The source file is as

```
/* Header and .Object files included in project are as: */

#include <windows.h>
#include "decl-32.h"
#include <stdio.h>

void GpibError(char *msg);      /* Error function declaration          */
int Device = 0;                 /* Device unit descriptor              */
int BoardIndex = 0;             /* Interface Index (GPIB0=0,GPIB1=1,etc.) */

void main() {
```

```
  int  PrimaryAddress = 2;        /* Primary address of the device        */
  int  SecondaryAddress = 0;      /* Secondary address of the device      */
  char Buffer[101];               /* Read buffer                          */

/* Initialization - Done only once at the beginning of application.*/

  Device = ibdev(                 /* Create a unit descriptor handle      */
      BoardIndex,                 /* Board Index (GPIB0 = 0, GPIB1 = 1, ...) */
      PrimaryAddress,             /* Device primary address               */
      SecondaryAddress,           /* Device secondary address             */
      T10s,                       /* Timeout setting (T10s = 10 seconds)  */
      1,                          /* Assert EOI line at end of write      */
      0);                         /* EOS termination mode                 */
  if (ibsta & ERR) {              /* Check for GPIB Error                 */
    GpibError("ibdev Error");
  }
  ibclr(Device);                  /* Clear the device                     */
  if (ibsta & ERR) {
    GpibError("ibclr Error");
  }

/****************** Main Application Body ********************/

  ibwrt(Device, "*IDN?", 5);  /* Send the identification query command  */
  if (ibsta & ERR) {
    GpibError("ibwrt Error");
  }
  ibrd(Device, Buffer, 100);    /* Read up to 100 bytes from the device   */
  if (ibsta & ERR) {
    GpibError("ibrd Error");
  }

  Buffer[ibcntl] = '\0';          /* Null terminate the ASCII string      */
  printf("%s\n", Buffer);         /* Print the device identification      */

/***Uninitialization - Done only once at the end of application.***/

  ibonl(Device, 0);               /* Take the device offline              */
  if (ibsta & ERR) {
    GpibError("ibonl Error");
  }
 ibonl(BoardIndex, 0);            /* Take the interface offline           */
  if (ibsta & ERR) {
    GpibError("ibonl Error");
  }
}
```

```
/*****************************************************************
 *                  Function GPIB ERROR
 * This function will notify you that a NI-488 function failed by
 * printing an error message.  The status variable IBSTA will also be
 * printed in hexadecimal along with the mnemonic meaning of the bit
 * position. The status variable IBERR will be printed in decimal
 * along with the mnemonic meaning of the decimal value.  The status
 * variable IBCNTL will be printed in decimal.
 *
 * The NI-488 function IBONL is called to disable the hardware and
 * software.
 *
 * The EXIT function will terminate this program.

*****************************************************************************
*****/
void GpibError(char *msg) {

   printf ("%s\n", msg);
   printf ("ibsta = &H%x  <", ibsta);
   if (ibsta & ERR )  printf (" ERR");
   if (ibsta & TIMO)  printf (" TIMO");
   if (ibsta & END )  printf (" END");
   if (ibsta & SRQI)  printf (" SRQI");
   if (ibsta & RQS )  printf (" RQS");
   if (ibsta & CMPL)  printf (" CMPL");
   if (ibsta & LOK )  printf (" LOK");
   if (ibsta & REM )  printf (" REM");
   if (ibsta & CIC )  printf (" CIC");
   if (ibsta & ATN )  printf (" ATN");
   if (ibsta & TACS)  printf (" TACS");
   if (ibsta & LACS)  printf (" LACS");
   if (ibsta & DTAS)  printf (" DTAS");
   if (ibsta & DCAS)  printf (" DCAS");
   printf (" >\n");

   printf ("iberr = %d", iberr);
   if (iberr == EDVR) printf (" EDVR <DOS Error>\n");
   if (iberr == ECIC) printf (" ECIC <Not Controller-In-Charge>\n");
   if (iberr == ENOL) printf (" ENOL <No Listener>\n");
   if (iberr == EADR) printf (" EADR <Address error>\n");
   if (iberr == EARG) printf (" EARG <Invalid argument>\n");
   if (iberr == ESAC) printf (" ESAC <Not System Controller>\n");
   if (iberr == EABO) printf (" EABO <Operation aborted>\n");
   if (iberr == ENEB) printf (" ENEB <No GPIB board>\n");
   if (iberr == EOIP) printf (" EOIP <Async I/O in progress>\n");
```

```
    if (iberr == ECAP) printf (" ECAP <No capability>\n");
    if (iberr == EFSO) printf (" EFSO <File system error>\n");
    if (iberr == EBUS) printf (" EBUS <Command error>\n");
    if (iberr == ESTB) printf (" ESTB <Status byte lost>\n");
    if (iberr == ESRQ) printf (" ESRQ <SRQ stuck on>\n");
    if (iberr == ETAB) printf (" ETAB <Table Overflow>\n");

    printf ("ibcntl = %ld\n", ibcntl);
    printf ("\n");
    ibonl (Device,0); /* Call ibonl to take the device and interface offline */
    ibonl (BoardIndex,0);
    exit(1);
}
```

The output of the above software is shown in the figure 4.4

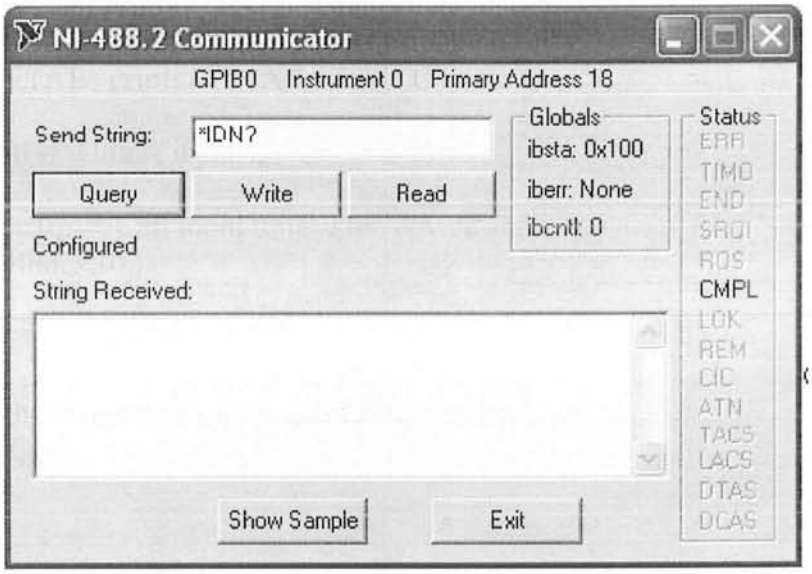

Figure 4.4

4.6.5 Rate Window

This system measures and stores complete capacitance transients together with the temperature and the basic capacitance values as the primary data file. According to manufacturer, Capacitance meter has response time 20 readings per second so 50 ms are required for one reading. We can not record any reading in time less than 50 ms. Experiments have revealed that practically the response time of the capacitance meter is round about 78 ms. Response time of the PC is 1 ms. The 2-points rate window can only be applied to the testing signal of frequency less than 10 Hz with pulse width of 0.5 ms with out coupling circuit. The capacitance meter can not detect filling pulse of width less than 0.5 ms due to capacitance bridge. To over come this difficulty coupling circuit is used by which filling pulse of 100 ns can be applied on sample. The whole capacitance transient is recorded for testing signal. The maximum (C_1) and minimum (C_2) values are sorted out from the transient, then the difference $\Delta C = C_1 - C_2$ of these values is calculated. Remaining values are thrown away.

4.7 Main Control Pannel

The main contol panel is consisted of the four subpanels:

- External Bias Parameters Panel
- Capacitance Meter Bus Mnemonics Panel
- Tempaerature control Panel
- Display Panel

4.7.1 External Bias Parameters Panel

This part of the software controls the parameters of the Pulse Generator. First the pulse generator is initialized by the above said NI-488.2 software then different parameters of the pulse generator are applied througth this control panel. This control panel is coded using the Common and Special sets of commands designed by Agilent. Through this control panel, we can apply frequency with prefixed increment and time interval upto upperfixed frequency limit to the sample for DLTS measurements. Pulse

width, amplitude, delay and offset can be adjusted through software for DLTS measurements. The major problem of synchronization of capacitance meter and pulse generator is solved by using two GPIB Cards and programming techniques. Both pulse generator and capacitance meter are functioning with out any delay. This panel is shwon in figure 4.5

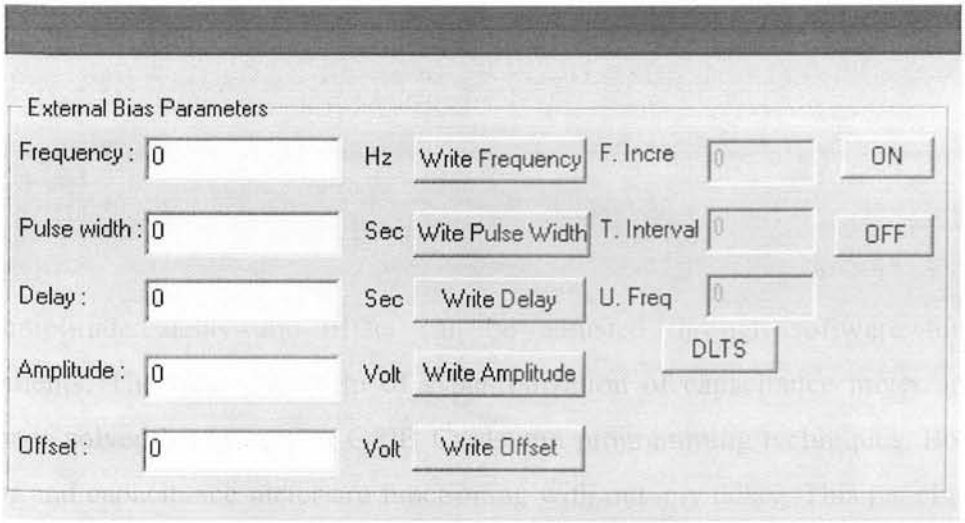

Figure 4.5

4.7.2 Capacitance Meter Bus Mnemonics Panel

All parameters of the capacitance meter can be applied throught this control panel. Similarly to pulse generator, capacitance meter is first initiallized then any bus mnemonic can be applied for certain function. Bus Mnemonics of the capacitance merter are divied into five groups. Any group of bus mnemonic can be selected and applied. Data can be entered through data entry table. The write, read and stop operations are controlled througth write, read, and stop buttons respectivily. There is a numeric display which display the current reading of the capacitance meter. There is also a counter. This counter counts and displays the readings of the capacitance meter. This panel is shown in figure 5.6.

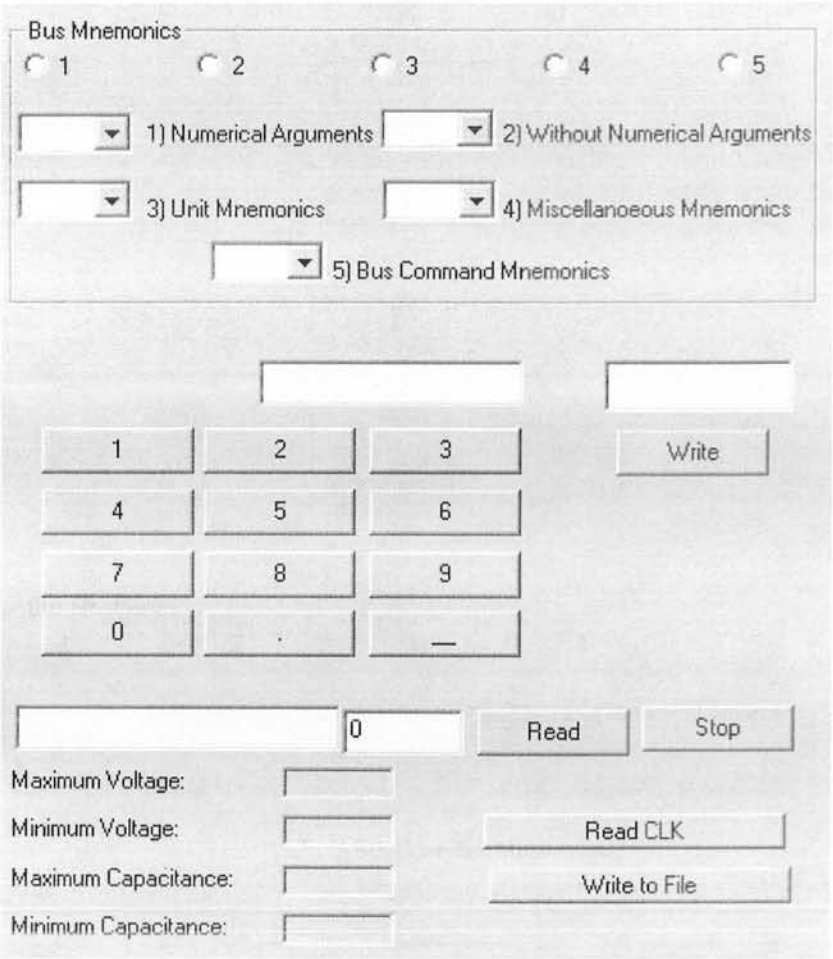

Figure 4.6

4.7.3 Temperature Control Panel

Temperature can be measured through Multimeter 2002 of Keithey. After initialization of the Multimeter, the measurement of temperature through scaning card can be configured by this panel. The emf of thermocouple can also be measured. Temperature can be set for maximum and minimum ranges. The measured temperature or emf of thermocouple can be stored in a file with capacitance transients. This contorl panel can be used to control the temperature controller. This panel is shown in figure 4.7

4.7.4 Display Panel

There are two display windows. One window displays the applied votlages at the sample. So we can observe wheather the voltages are applied or not at the sample. Second window displays the capacitance response of the capacitance meter. We can

observe the change in capacitance transient with temperature at any time. This panel is shown in figure 4.8

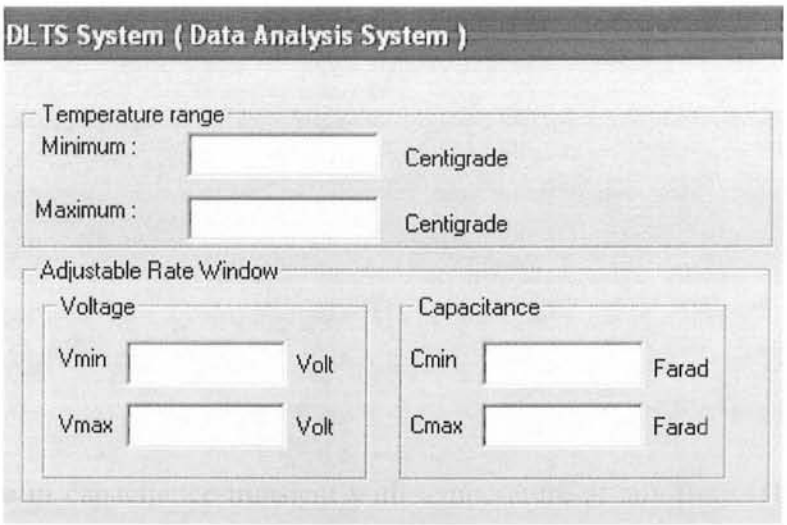

Figure 4.7

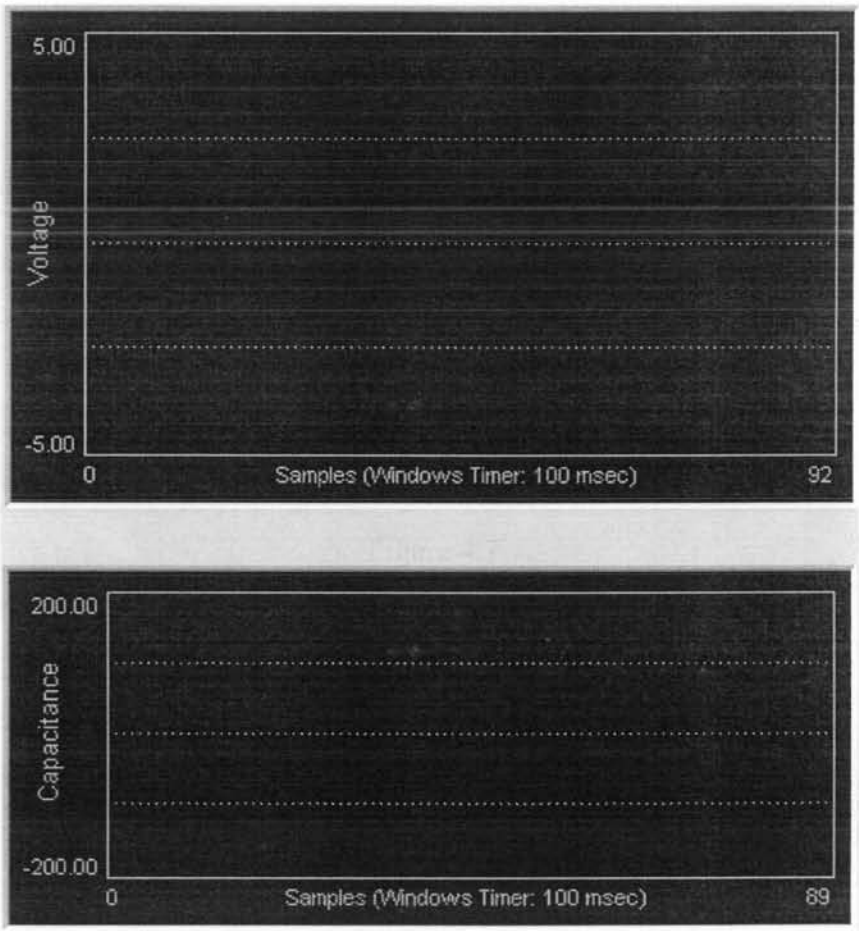

Figure 4.8

References:

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CHAPTER

5

Experimental Details

5.1 Introduction

This chapter provides the information about the experimental work carried out in laboratory. The experimental work can be divided into two parts. First part is concerned with measurements taken with our home made digital computerized DLTS and second part is about measurements taken by using company made DLTS system. Possibilities of improvements of the digital computerized DLTS are also discussed in this chapter. Thermally induced defects in device during fabrication are discussed. In the 2nd part thermally induced defects usually introduced by rapid quenching of the material (in diffusion pump oil, water and glycerol or simply in air) from high temperatures to room temperature are studied. Quenched in defects are normally attributed to transition metals present inadvertently or to their complexes in semiconductor materials especially in silicon. In addition, the data obtained is analyzed, compared with the literature and results are discussed at length.

5.2 Sample Preparation

The samples were prepared under different conditions for this research work. The samples were p^+n diodes. They were fabricated on n-type vapour phase epitaxial silicon grown on p^+ substrate. The p^+ top layers were obtained by the implantation of boron and phosphorus, respectively. The resistivity of the silicon was 6.5 to 8.5 Ω-cm for p-type.

The substrate material used in the preparation of all the diodes was Czochralski grown. The conditions used during preparation of samples are given in Table5.1

After heat treatment and quenching, diodes were cleaned and washed by routine procedures. After going through cleaning procedure the samples were dried. Ohmic contacts were made on the back surface of the diode by rubbing Gallium with Aluminum rod to produce a Ga-Al layer, which is known to serve as good ohmic contact to silicon down to cryogenic temperature. The diodes were then mounted on TO-5 headers with conducting silver epoxy on a metallic plate which is fixed to TO-5 header with non conducting epoxy. The top connections were made with aluminum wire bounded ultrasonically to the diode and the leads of the TO-5 header.

Serial #	Diode	Quenched Temperature	Time for Quenched	Quenched in
D1	p^+n	Virgin	-	-
D2	P^+n	850 ^{0}C	2.5 hours	air
D3	P^+n	1250 ^{0}C	2 hours	air

Table 5.1

5.3 Current–Voltage (I-V) Measurements

Current-voltage characteristics are very important for further investigation of a sample at certain temperature. These measurements of sample reveal important information about the suitability of sample for DLTS measurements. The information is useful for data analysis of the results. The current – voltage (I-V) characteristics of each diode were studied using digital electrometer (Advantest Model # TR8652). This digital electrometer can measure current upto Pico Ampere. The reverse leakage current for diode was measured at 300 K, 273 K and 77 K. The reverse leakage currents in all the diodes selected for characterization of deep levels ranged from ~ 1μA to 300 nA at -3V. The typical reverse bias (-3V) is used during the experiments for measurement of the deep levels characteristics. The reverse leakage currents in this range are low enough for meaningful and accurate DLTS measurements. The theory of current-voltage

characteristics has been explained in chapter 3. If the diode voltage $V_R >> nKT$, then equation of current through diode is as follow:

$$I = I_0 \exp\left(\frac{qV_R}{n\,kT}\right) \qquad 5.1$$

The equation 5.1 can be written in linear form by taking the log on both sides of this equation. The linear form of the equation 5.1 is given as:

$$\ell n\,(I) = \ell n\,(I_0) + \left(\frac{qV_R}{nkT}\right) \qquad 5.2$$

This is equation of straight line. We can calculate ideality factor n from the slope of this line. The value of ideality factor n determines which type of current dominates. If the value of $n = \sim 1$, then diffusion current dominates. If the value of $n = \sim 2$, then recombination current dominates. If $1 < n < 2$ then both currents are present, where $\ell n\,(I_0)$ is the intercept of this line. A plot between $\ell n\,I$ and applied reverse voltage V_R of diode gives a straight line. We calculate the ideality factor n from the slope of this straight line. The figure 5.1 and figure 5.2 represent the plots between I and applied voltage Vr at 300 K and 77 K respectively. The plots between $\ell n\,I$ and Vr at 300 K and 77 K are shown in figure 5.3 and figure 5.4 respectively.

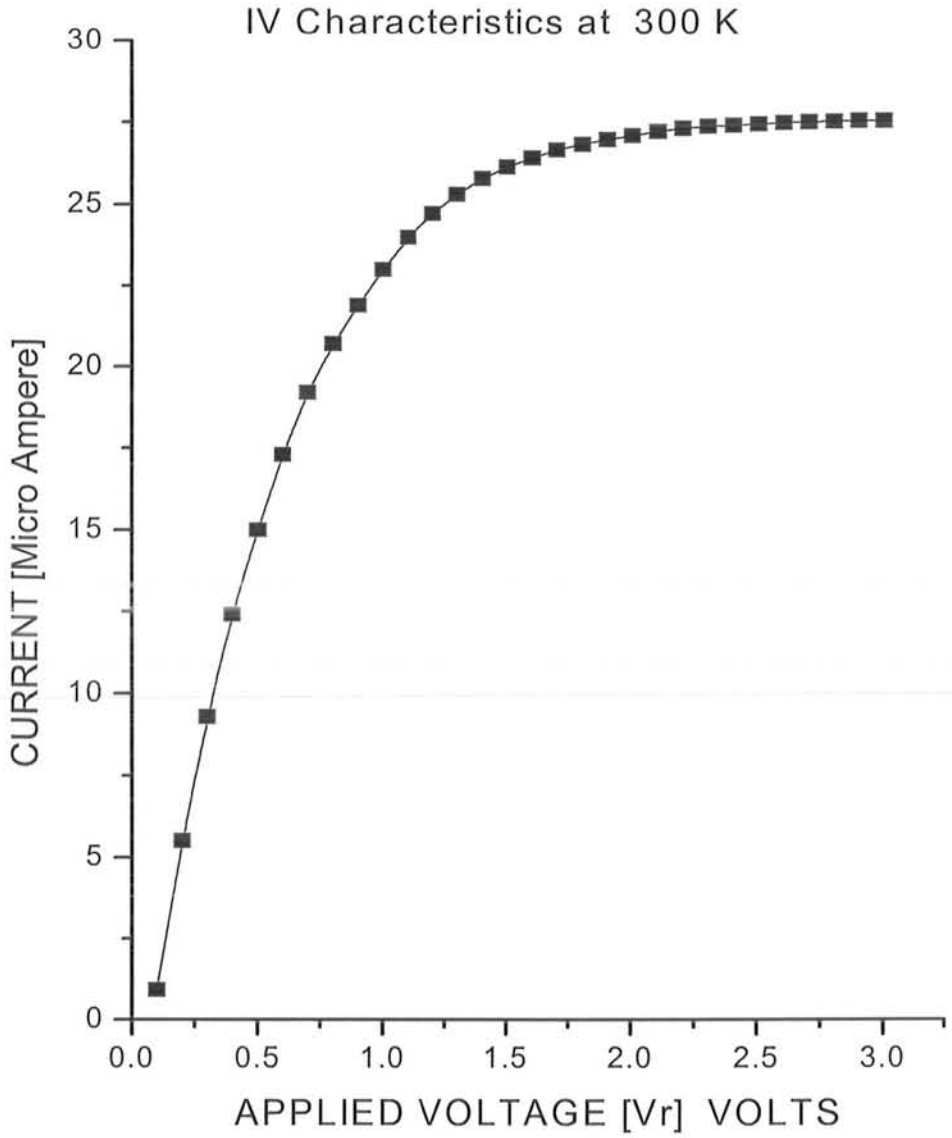

IV Characteristics at 300 K
CURRENT [Micro Ampere]
APPLIED VOLTAGE [Vr] VOLTS
0
5
10
15
20
25
30
0.0
0.5
1.0
1.5
2.0
2.5
3.0

Figure 5.1

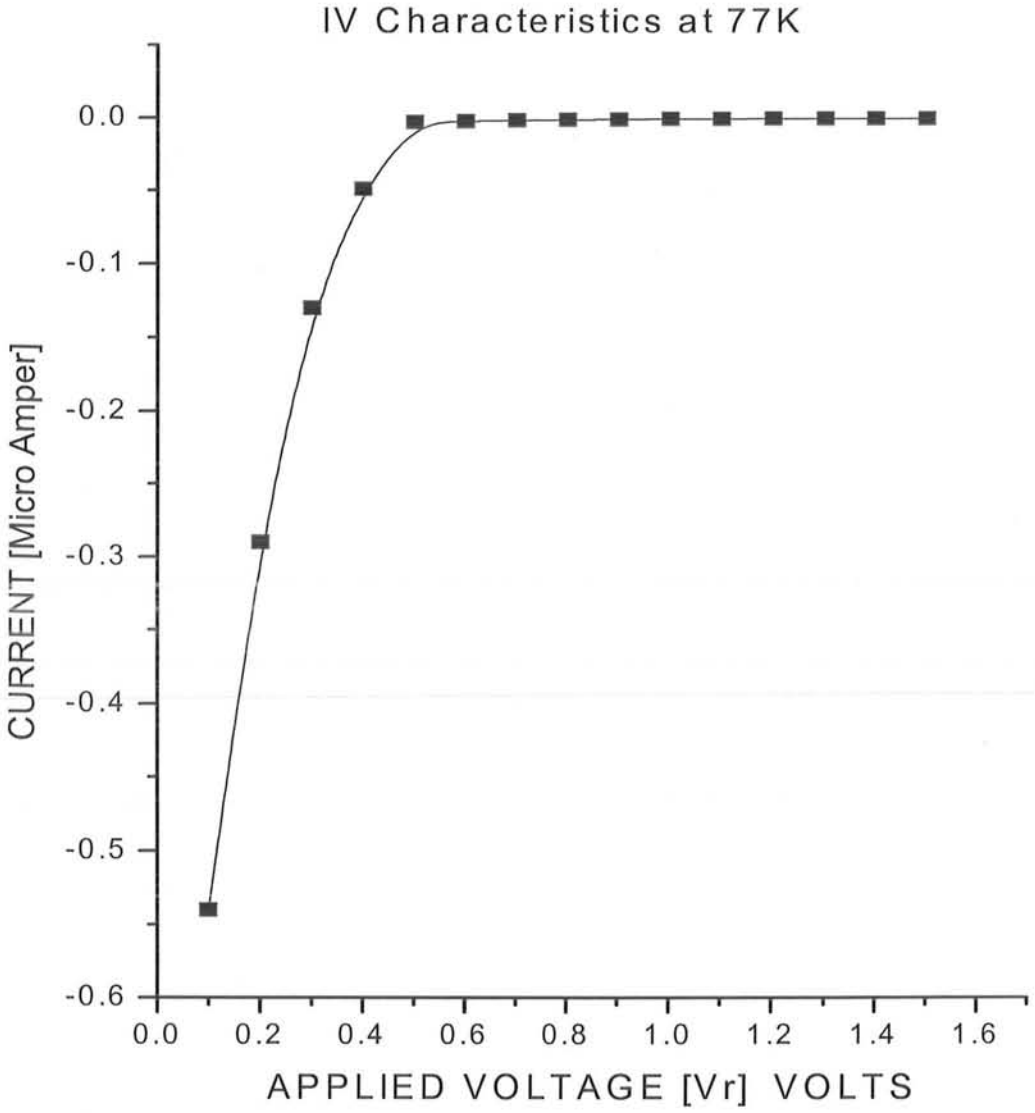

IV Characteristics at 77K
CURRENT [Micro Amper]
0.0
-0.1
-0.2
-0.3
-0.4
-0.5
-0.6
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
APPLIED VOLTAGE [Vr] VOLTS

Figure 5.2

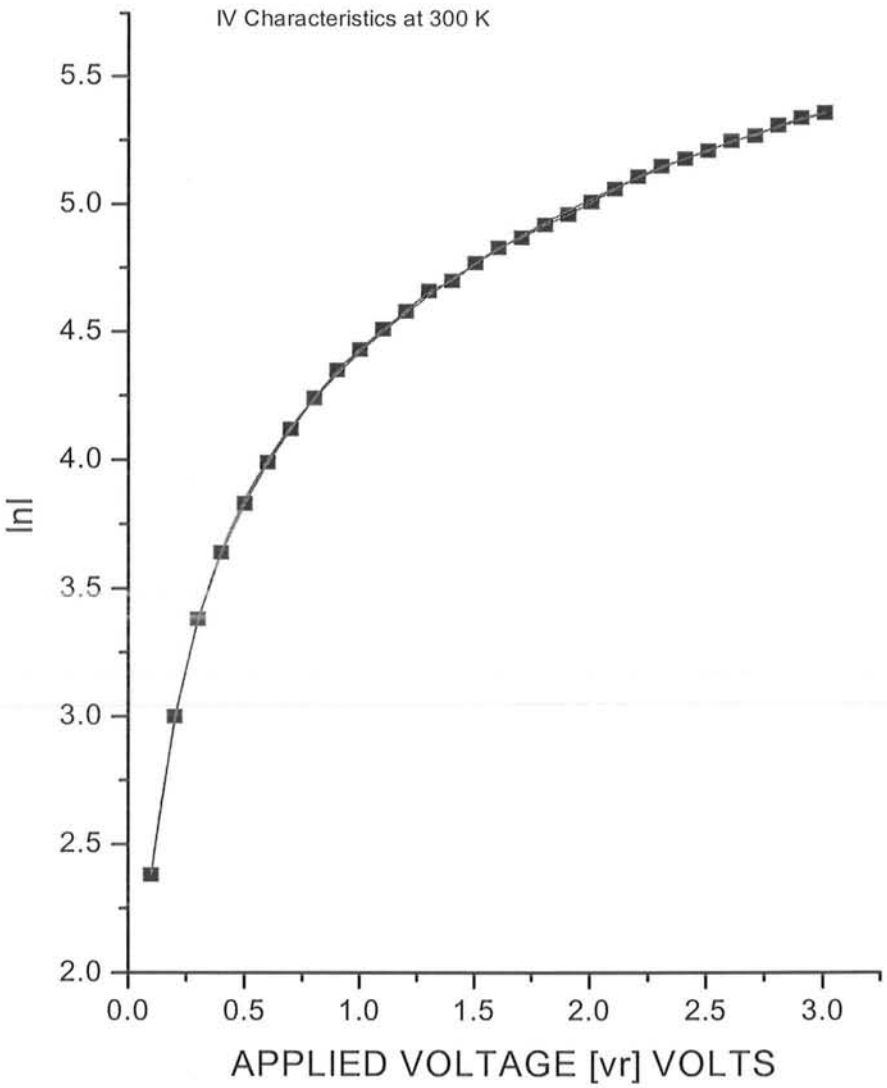
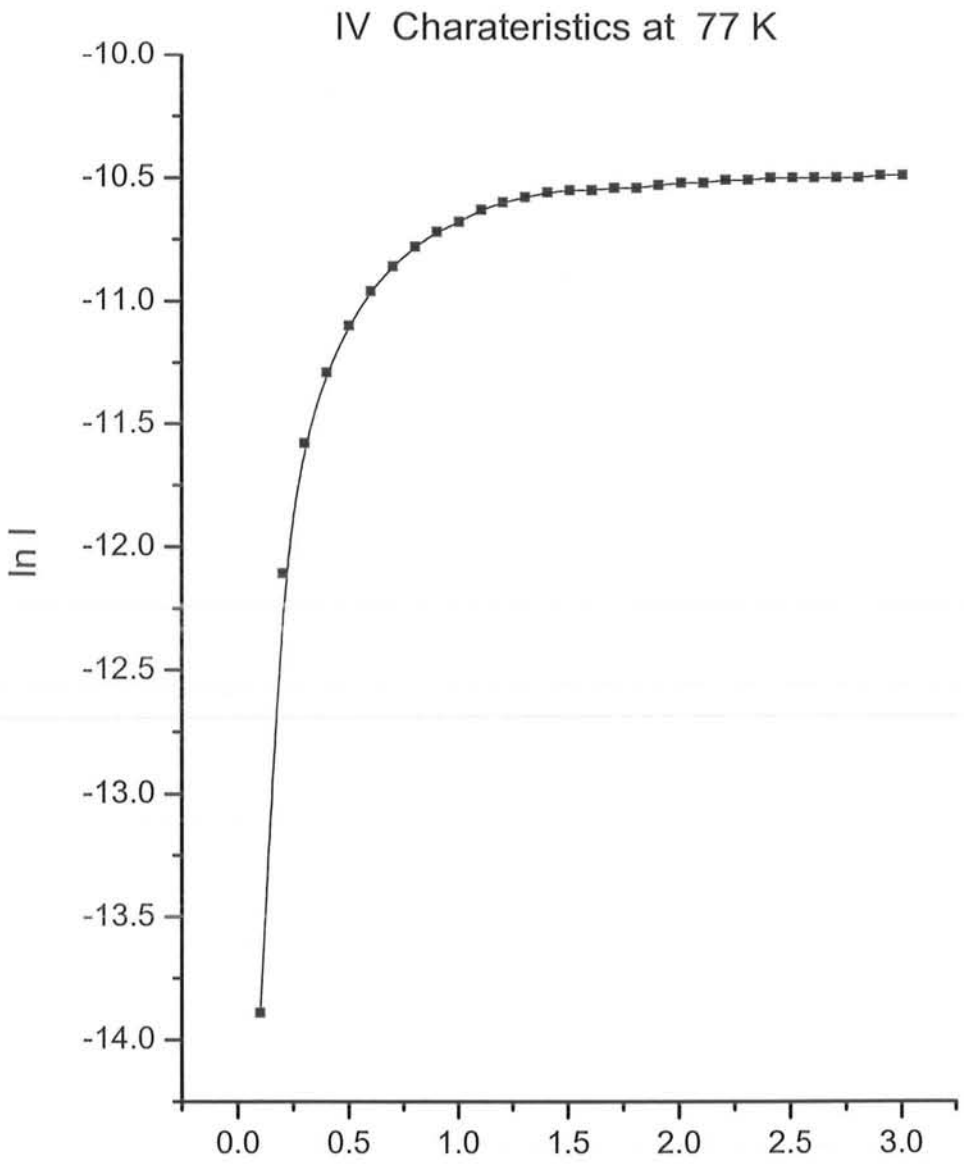

IV Characteristics at 300 K
5.5
5.0
4.5
4.0
3.5
3.0
2.5
2.0
|n|
0.0
0.5
1.0
1.5
2.0
2.5
3.0
APPLIED VOLTAGE [vr] VOLTS

Figure 5.3


IV Charateristics at 77 K
-10.0
-10.5
-11.0
-11.5
-12.0
-12.5
-13.0
-13.5
-14.0
ln I
0.0
0.5
1.0
1.5
2.0
2.5
3.0
APPLIED VOLTAGE [Vr] VOLTS
Figure 5.4

5.4 Capacitance –Voltage (C-V) Measurements

Capacitance – voltage characteristics determine the dopant concentration and doping profile of the diode. These information are needed to obtain the deep-level defect concentration and their profiles from the DLTS data. Capacitance – voltage measurements conveniently provide us the information. Capacitance-voltage characteristics also provide us information about the nature of the junction. The junction is abrupt if the quantity $1/C^2$ varies linearly with applied reverse voltage Vr. The junction is linearly graded if the quantity $1/C^3$ is directly proportional to the applied reverse voltage Vr. These information help in interpretation of the results from the DLTS scan

The doping concentration N_a and N_d for p-n junction were calculated from this expression

$$C = \varepsilon A \left[\frac{q}{2\varepsilon(V_0 - Vr)} \left(\frac{N_a N_d}{N_a + N_d} \right) \right]^{1/2} \qquad 5.3$$

Where, C is the capacitance of the junction at a reverse applied voltage Vr. A is the area of the junction. q is the charge of the depletion region. N_a and N_d are the concentrations of the acceptor and donor impurities.

If the junction is asymmetrically doped then the transition region lies primarily into the less heavily doped side, and the capacitance is determined by only one of the doping concentrations. For a $p^+ n$ junction the capacitance is given as follow:

$$C = A \left[\frac{\varepsilon q \ N_d}{2 (V_0 - Vr)} \right]^{1/2} \quad \text{For } p^+n \qquad 5.4$$

It is possible to measure the concentration of the lightly doped region from a measurement of junction capacitance using the equation

The C-V characteristics of each diode were measured by using a sensitive Boonton capacitance meter model 7200 at 300 K and 77 K. Boonton capacitance meter is connected to PC through GPIB card. Boonton capacitance meter is automatically controlled through software which is coded in Visual C++. These plots are drawn between capacitance (pF) and applied reverse voltage Vr (Volts) at 300 K and 77 K as shown in figure 5.5 and figure 5.6 respectively. The graphs between 1/ C^2 and applied reverse voltage Vr are drawn at 300 K and 77 K as shown in figure 5.7 and figure 5.8 respectively.

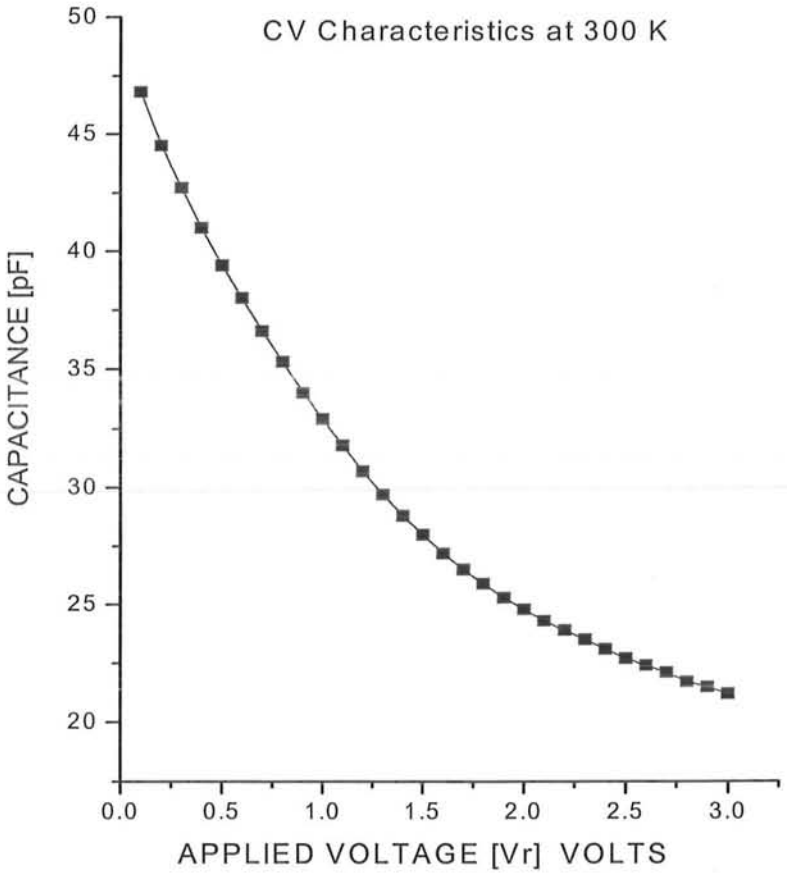


Figure 5.5

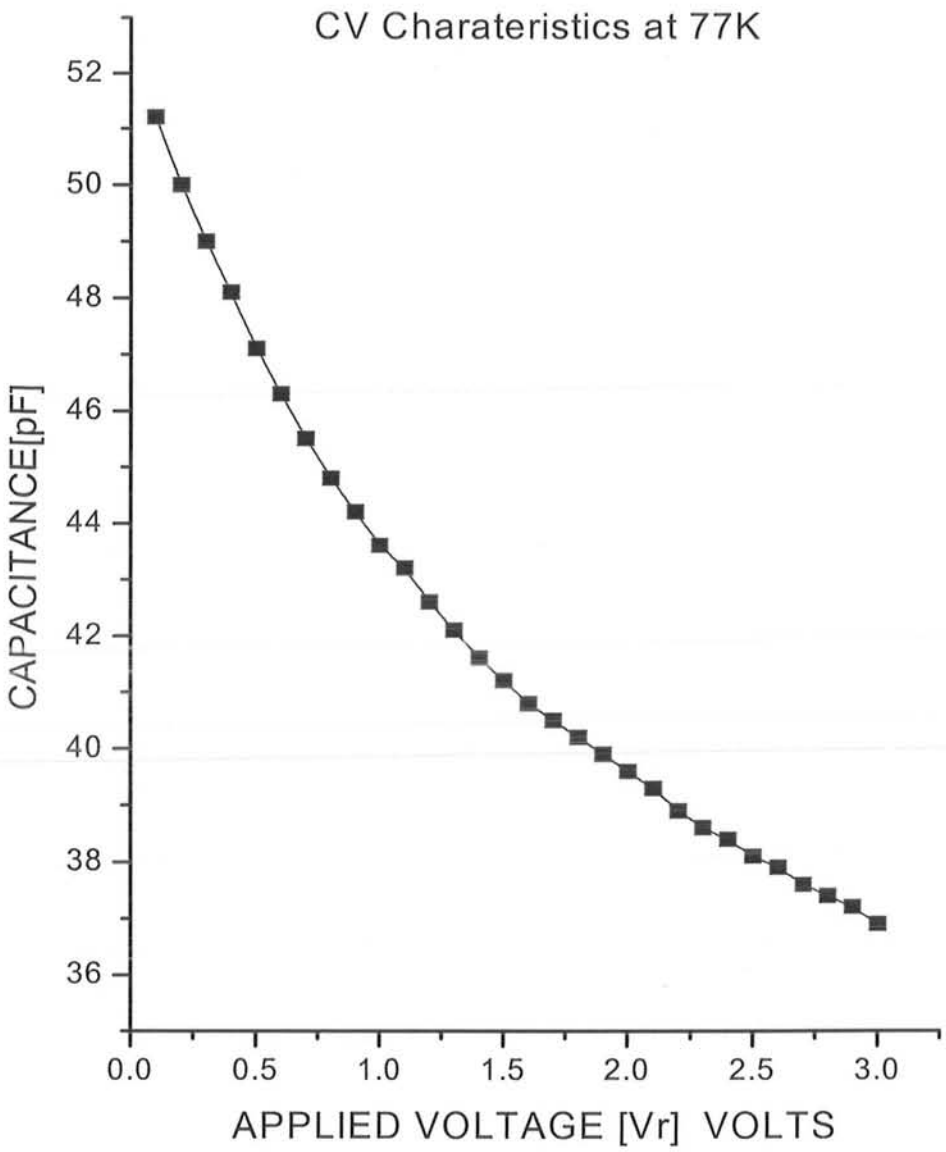

CV Charateristics at 77K
CAPACITANCE[pF]
52
50
48
46
44
42
40
38
36
0.0
0.5
1.0
1.5
2.0
2.5
3.0
APPLIED VOLTAGE [Vr] VOLTS

Figure 5.6

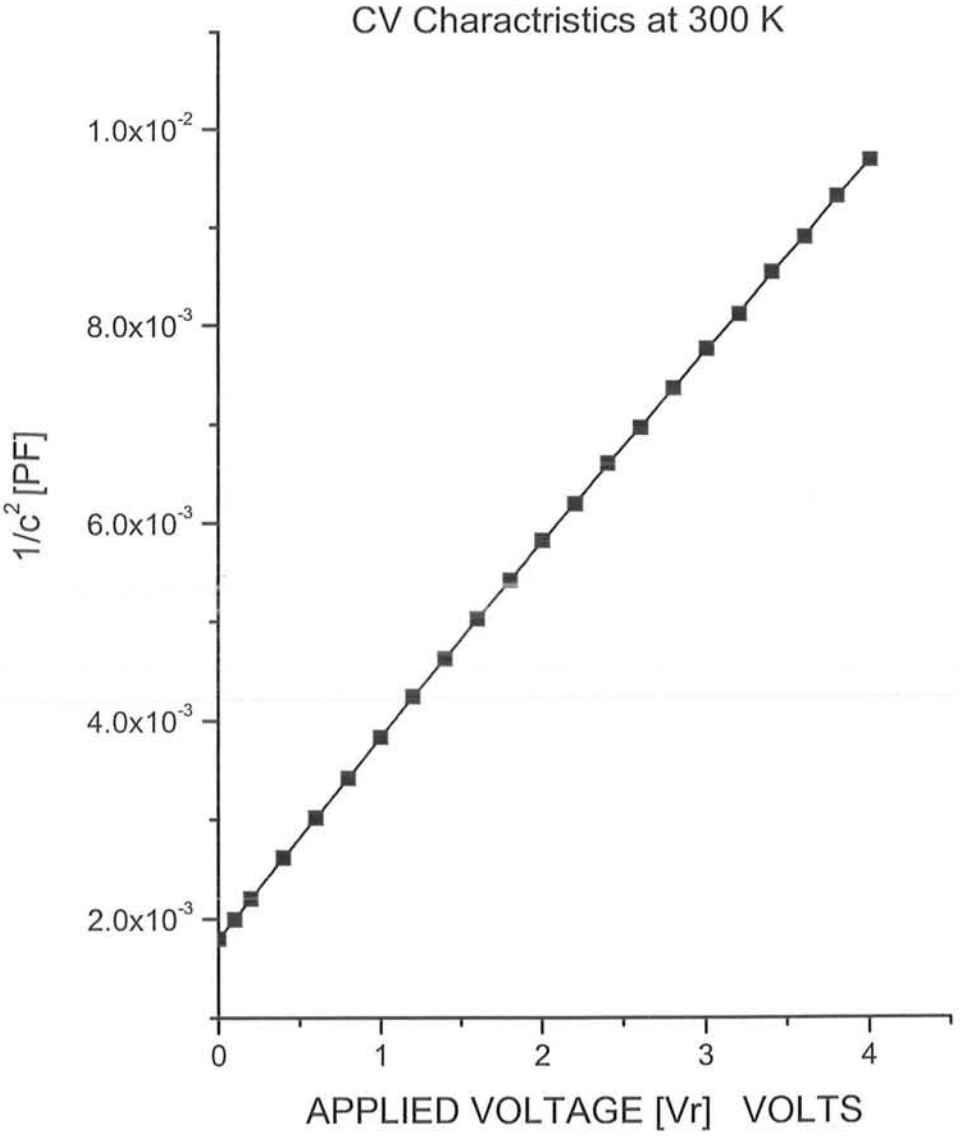
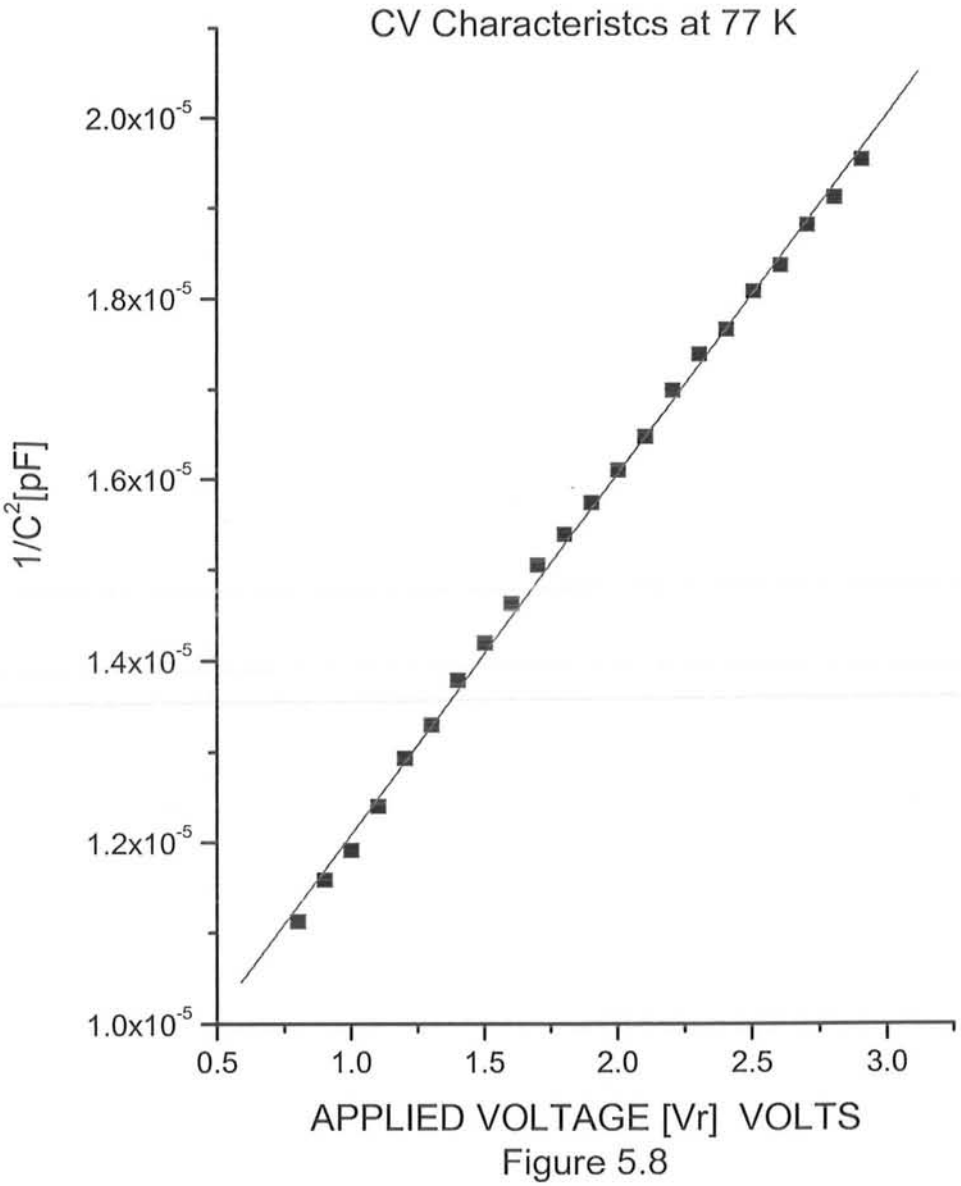

CV Charactristics at 300 K
1.0x10-2
8.0x10-3
6.0x10-3
4.0x10-3
2.0x10-3
1/c2 [PF]
0
1
2
3
4
APPLIED VOLTAGE [Vr] VOLTS

Figure 5.7


CV Characteristcs at 77 K
2.0x10-5
1.8x10-5
1.6x10-5
1.4x10-5
1.2x10-5
1.0x10-5
1/C2[pF]
0.5
1.0
1.5
2.0
2.5
3.0
APPLIED VOLTAGE [Vr] VOLTS
Figure 5.8

5.5 Single-Shot Measurements

The essential physics of all form of thermally stimulated space-charge spectroscopy (like DLTS) is based on the thermal-emission transient at some fixed temperature. The techniques which have the benefits of speed and convenient to use for the study of the complex trap spectra, but they cannot produce raw data of any higher quality than can be done with a large number of isothermal transients recorded at many different temperature.

Isothermal capacitance transients were first proposed as a technique to study traps in semiconductors by Williams [1], Furukawa and Ishibashi [2].The qualitative and quantitative description of single-shot technique is discussed in chapter 3.

A capacitance transient due to majority-carrier emission is always negative and due minority-carrier emission is always positive.

The activation energy $E = E_c - E_T$ for electrons emission or $E_A = E_T - Ev$ for hole emission can be calculated from the slope of an Arrhenius plot. i.e. a plot of log of the transient decay rate $\alpha+\alpha^*$ as a function of 1/T.Where T is the absolute temperature at which the transient is recorded. This follows from the relationships

$$\alpha = \nu \exp (-E/kT) \qquad 5.5$$

$$\alpha^* = \nu^* \exp (-E_A^*/kT) \qquad 5.6$$

It is fact that either α or α^* usually dominate the transient rate. The activation energy measured in this way is a valid parameter of the trap, but it may not be the true depth of the trap.

The single-shot measurements are taken in our laboratory. The measurements are taken at applied reverse voltage (Vr = -3V) at 300 K, 273 K and 77 K. It is already mentioned that temperature could not be controlled precisely due to unavailability of temperature controller. The transients obtained from our digital computerized single shot technique have large value of signal-to-noise ratio (SNR). This is due to digital behaviour of Boonton Capacitance meter and response time of Boonton Capacitance meter and PC system. Single-shot measurements are taken through PC controlled by the software. The graph is drawn between compensated ΔC and time t. The noisy graphs are improved by regression methods. The figure 5.9 (a), (b), figure 5.10 (a), (b) and figure 5.11 (a), (b) are transients recorded at 300 K, 273 K and 77 K.

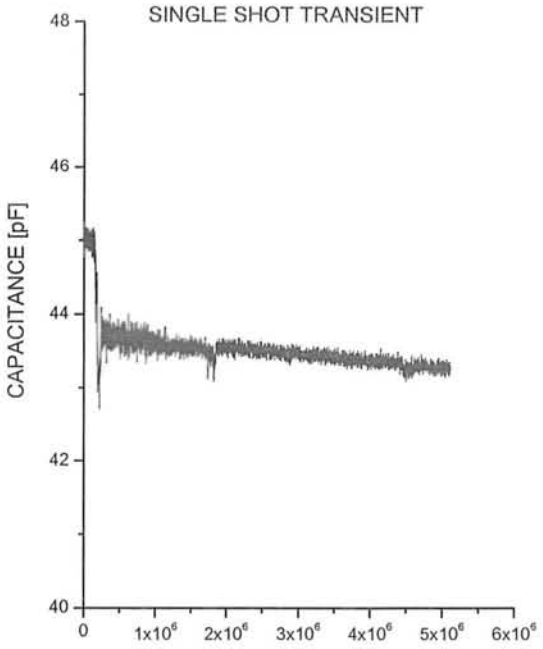


Figure 5.9 (a)

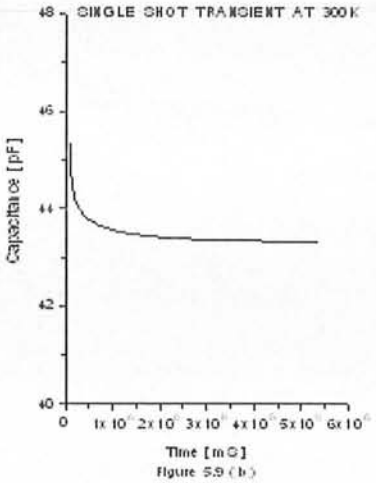


Figure 5.9 (b)

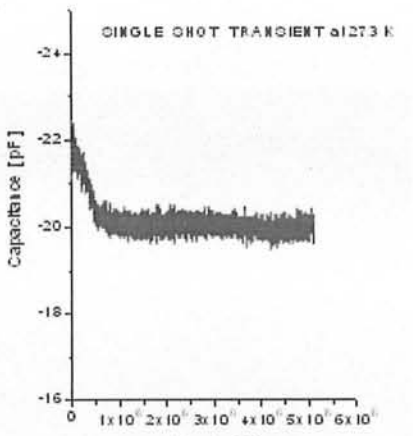


Figure 5.10 (a)

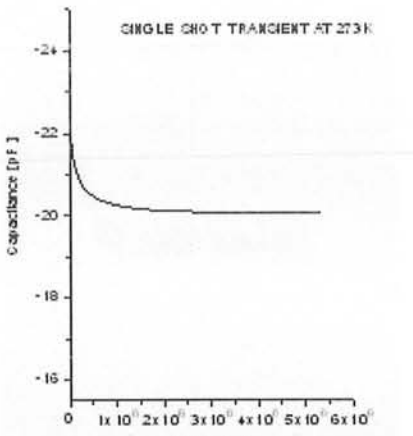


Figure 5.10(b)

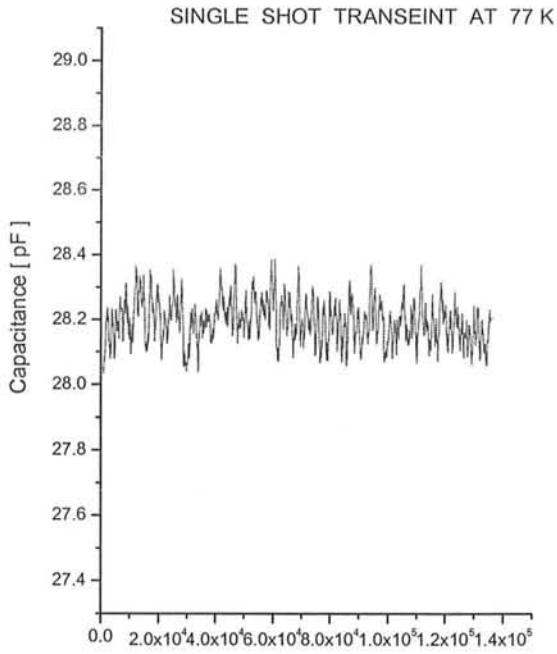


Figure 5.11 (a)

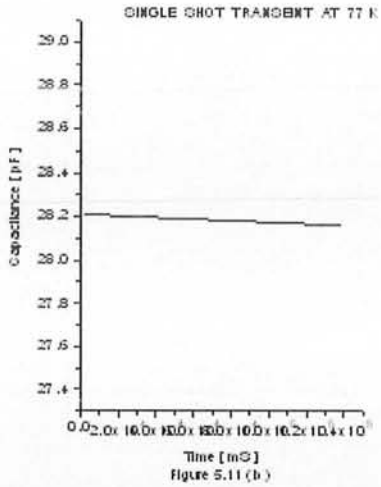


Figure 5.11 (b)

5.6 DLTS Measurements

The basic idea of the DLTS technique is the rate-window concept. If we consider a train of repetitive bias pulses applied to the sample, we then have a signal which consists of a series of transients with a constant repetition rate. As the temperature is varied, the time constant of the transient varies exponentially with 1/T, where T is absolute temperature at which the transient is recorded.

A DLTS spectrum looks superficially like the signals produced by the single-shot technique. However, there are several important differences. First, the DLTS scan is reversible and does not depend on fixed temperature. Thus one can scan up or down in a temperature range at any rate and can even stop the scan on a peak to study the capture properties or spatial profile of that particular trap. Another advantage is that the baseline is always flat. It means that there is good common-mode rejection of the steady-state capacitance variations.

The depth of the deep-level in a sample is calculated by determining the activation energy of that level. The best way to determine the activation energy of the deep level is to construct an Arrhenius plot. This can be done simultaneously for nearly all of the traps in a sample by recording several DLTS spectra using different rate windows. An Arrhenius plot is constructed by plotting the log of rate window verses the inverse temperature of the DLTS peak T_m^{-1}.

A very rough measure of the activation energy of the trap may be estimated directly from the temperature T_m of the maximum of the DLTS peak. This is analogous to the determination of energies from TSC peak position according to equation 5.7. Buehler and Phillips [3] have analyzed TSC and TSCAP experiments and have shown that the temperature T_m of the TSC maximum or midpoint of the TSCAP step is related to the activation energy as

$$E = kT_m \ln \{ (\nu\, kT_m^2)/ q(E + 2\, kT_m)\} \qquad 5.7$$

If we assume that $\nu = 10^{12}$ s^{-1}, then with a rate window of $\tau^{-1}_{max} = 50$ s^{-1}

We find $E \approx 23.7\, kT_m$. Since E depends only logarithmically on ν, this temperature-energy conversion is accurate to approximately $\pm 10\%$.

DLTS scans are taken with our home made digital computerized DLTS system from 77 K to room temperature at applied reverse voltage Vr = -3V. The compensated capacitance was excluded from the spectrum in a typical scan as shown in figure 5.12. The filling pulse has the following parameters: frequency of pulse f = 9 Hz, pulse width t_p =10 ms, and amplitude was -3 V.

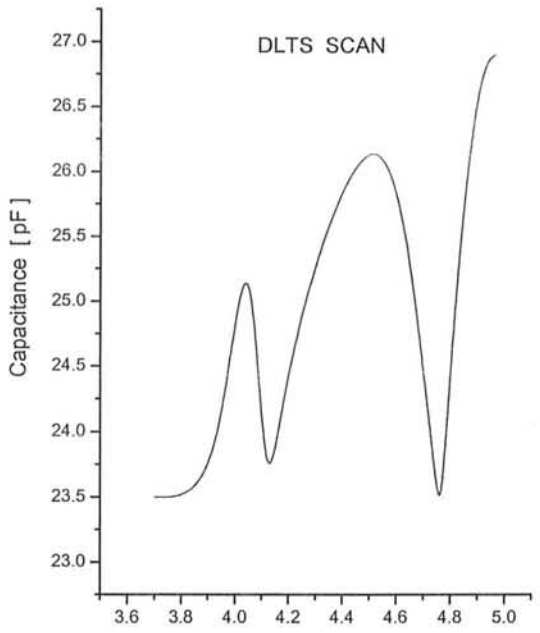


Figure 5.12

5.7 Measurements Using Company Made DLTS:

DLTS system developed in the laboratory can be used for a very small range frequency with out temperature controller. Precise measurement can not be taken even in this small frequency range. Keeping in view these short comings of computerized DLTS, measurements taken by using company made DLTS are presented, analyzed and discussed in the coming sections.

A routine check up of I-V and C-V characteristics has been carried out for the selection of suitable diodes for further measurements.

Deep level transient spectroscopic technique (DLTS) has been employed to study the defects induced by quenching. Typical DLTS scans of virgin sample (D1) and quenched samples D2 and D3 are shown in figure 5.13. The DLTS traces of Diodes D1, D2 and D3 are labeled as S1, S2 and S3 respectively.

5.7.1 Virgin Sample

Three small peaks named A, B, C are visible in the DLTS spectrum of a virgin sample (D1). The peaks labeled E and F are hardly visible in the spectrum.

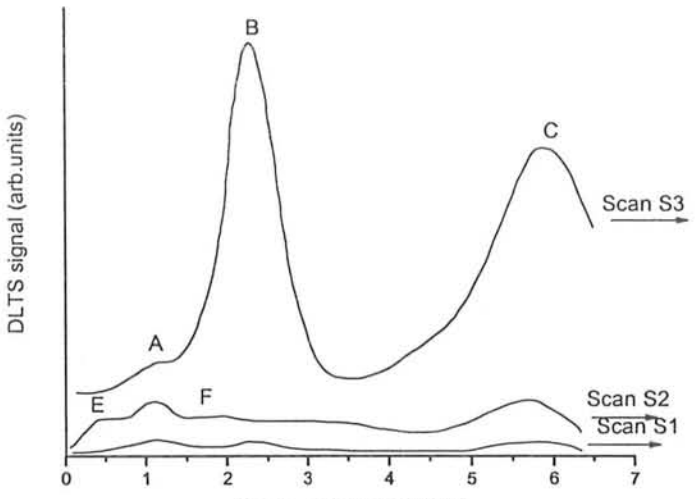


Figure 5.13

5.7.2 Air Quenched Samples

Five small peaks, named A, B, E, F and C, are observed in the DLTS scan S2 of Sample D2. The concentrations of the defects assigned to peaks A, E and C, as is clear from the peak heights, were found comparable to each other though not very high. The peak heights of B and F are very small rather invisible. The DLTS scans of sample D3 are significantly different from the scans of samples D1 and D2. Only two dominant peaks B and C are observed in the scan. Due to significant increase in heights of the peaks B and C all other peaks observed in scans S1 and S2 could not show themselves or they are suppressed at high temperature heat treatment. However peak A is visible but with very low concentration.

5.8 Comparison of Samples Quenched in Air With Virgin Sample

Now for comparison of DLTS spectrum of air quenched samples the traces S2 and S3 are plotted in the same figure 5.13. The height of peaks A, C, E and F has been found increased slightly in the scan S2 as compared to the peaks in scan S1 of sample D2 (quenched in air from 850 °C). The peak B in scan S2 is not visible. Astonishingly Peaks B and C in DLTS scan S3 of a diode D3 quenched in air from 1250 °C have increased

approximately 40 and 20 times respectively. The position of peak C does not appear shifted as compared to its position in virgin sample.

5.9 Emission Rate Measurements

Emission rate signatures of defects/energy states related to peaks A, B and C has been measured. Peak heights of E & F are very small for the measurements of emission rate signatures. Therefore, no meaning full measurements could be performed on these defect states. Emission rate data of defect states A, B and C has been plotted on T^2 corrected Arrehenius plot as shown in figure 5.14. The activation energies obtained from the best fit lines through the data points plotted on T^{-2} corrected Arrehenius plots are E_c - 0.23 eV, E_c - 0.25 eV, and E_c - 0.55 eV respectively.

5.10 Isochronal Annealing

Isochronal annealing of the diode D3 has been performed in the nitrogen ambient from room temperature to higher temperature. Diode was heated at a fix temperature for ~25 minutes each time. The response of different levels appearing in DLTS spectrum of the diode D3 is discussed below. Annealing characteristics of both dominant levels B and C plotted in figure 5.15 show very interesting response of the defects to annealing temperature. The concentration of the level C remains nearly constant up to 175°C.

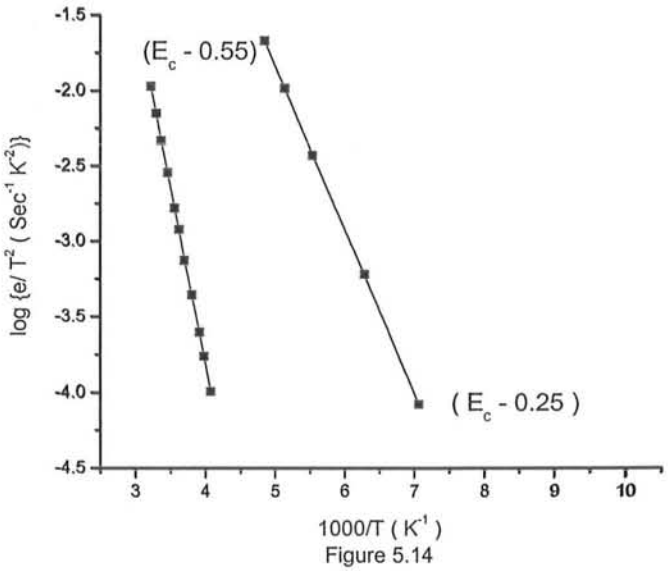


Figure 5.14

Beyond 175°C concentration increases up to 275°C and afterwards it again becomes constant. A similar behaviour of Energy state B has been observed. The increase in concentration of B starts a step earlier than the increase in concentration of C. A careful examination of the characteristics of B and C shows that there is hump in the characteristic curve of level B and a dip in the characteristics of level C. This hump and dip are appearing in between temperature 200°C and 275°C. The minima of the dip and the maxima of the hump appear at the same temperature.

This peak like behaviour in concentration of the defect has been reported by Brotherton (1984) [4] for iron related defect and trough like behaviour has been reported for gold related defect

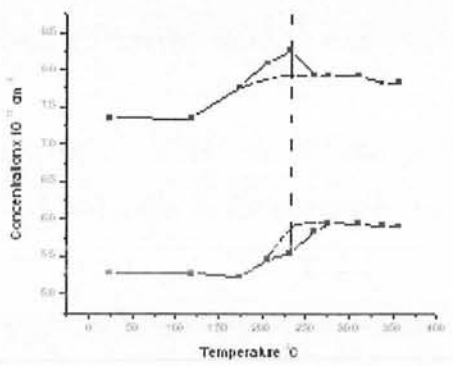


Figure 5.15

5.11 Discussion

The levels B and C are characterized in detail. Their characteristics and identification are discussed below.

5.11.1 Thermally Induced Deep Level C

DLTS spectra of air quenched samples p^+n D2 and D3 show that the defect assigned to electron emitting deep level C corresponding to peak C is found present in significant concentration in the quenched samples D2 and D3 while peak height in DLTS scan for virgin samples indicate a minor concentration of this level in virgin samples. The

highest concentration has been found in D3 samples which are heat treated at 1250°C for and then quenched in air.

Emission rate signatures of this level exactly fall on the emission rate signatures of Au (A) reported elsewhere. Its isochronal annealing characteristics corrected for (Fe) are similar to those measured for Au (A). Concentration of this level is similar to that observed in Au doped samples for Au (A) prepared under identical conditions reported in 1995. This suggests that sufficient inadvertent gold is present in these samples. We are therefore justified to identify this level as gold acceptor Au (A) at energy position E_c - 0.55 eV. All the samples are made from same wafer therefore one could expect similar concentration of this defect in all D1, D2 and D3 samples. But its concentration is very low in D1 and D2 samples and very high in D3 samples indicating that gold remains on electrically inactive sites at low temperatures but at higher temperatures it either appears on electrically active sites or forms a complex with other inadvertent impurities which then contribute to the signal.

5.11.2 Thermally Induced Deep Level B

The defect corresponding energy state (E_c -0.25) exists in virgin samples in low concentration but its concentration is very high in samples heat treated at 1250°C and then quenched in air. It is the dominating peak with very high concentration. The isochronal annealing characteristics show that the concentration of this defect remains nearly constant except with some minor variation between temperatures-125°C to 250°C. The variation in the concentration shown in annealing characteristics complements the response of iron signal in C. It may be due to gold component of the complex assigned to this peak. From the annealing characteristics this defect it is clear that this defect is very stable up to the temperature used for annealing. The overall response of the defect to annealing is similar to the response of defect assigned to C, now identified above as gold related level. This similarity in the response to annealing shows that this defect is pinned with energy state C or it can be proposed that this level is a different charge state of E(0.55) level.

The appearance of a dip and a hump and their complementary behaviour suggest the contribution of signal due to gold related level in peak C and contribution of iron related

defect in peak B. Similar annealing characteristics (corrected for iron and gold, dashed line in figure 5.15) of the defects related to B and C suggest that the signal due to Fe related level is responsible for the hump in the characteristics of the peak B and signal due to gold related level is responsible for the dip in annealing characteristics of the peak C. If the contributions of Au related level and Fe related levels are subtracted from the respective annealing characteristics of B and C, very interesting information is obtained. Dotted line shows the characteristics after subtraction of the signal due to Au and Fe related levels. After subtraction the response of the both levels to annealing temperature is very similar. Subtracted annealing characteristics clearly indicate that these two defects B and C are pinned together or they are two different charge states of the same defect.

5.12 Conclusion

A lot of work has been done to develop a computerized digital DLTS system. In addition this DLTS system a detailed work has also been carried out to study the quenched in iron related defects in silicon. Following are our main conclusions.

1 we successfully developed a computerized DLTS system which can work in a small range of frequency and pulse-width. Further improvements are suggested under topic work for future.

2 A detailed study on quenched in defects in silicon revealed two main quenched in levels at energy positions E_c -0.55 eV and E_c – 0.25 eV.

3 Annealing characteristics of these defects have been studied in detail. It is noted that these two defects are pinned together.

4 Energy position and annealing characteristics suggest that a level at E_c -0.55 eV is gold related complex while other level at energy position E_c – 0.25 eV is a complex of gold with iron.

5.13 Work Suggested for Future.

A digital computerized DLTS system has been developed in our laboratory. This digital computerized DLTS system is consisted of four main units. These units are capacitance meter, function generator, personal computer, and temperature controlling

unit. The capacitance meter and function generator are interfaced through two GPIB cards and these are controlled and run through a software. This software is programmed in visual C++. Temperature controlling unit has to be interfaced with PC and software has also to be coded for controlling temperature. Measurements have been taken by this digital computerized DLTS system. Our DLTS system no doubt can measure DLTS out put signal with in a short range of frequency and over a small range of temperature. We are looking for a temperature controller to have good control on temperature. This system still needs improvements in its hardware as well as in its software.

Enhancement in hardware is needed because the response time of the capacitance meter is not enough. Its digital output is not fast. These difficulties are because of capacitance bridge circuit of capacitance meter. Signal-to-Noise ratio (SNR) is also low. To overcome these difficulties, we have to change its analog output into digital form by an analog to digital converter (ADC) of better resolution than capacitance meter. This digital output of ADC is recorded and processed by software. Capacitance meter and function generator can be triggered in through a digital to analog converter (DAC). These difficulties can also be solved through application of data acquisition card. Clock of data acquisition card can be programmed for generation of pulses of required parameters.

Enhancement in software basically depends on the hardware enhancement. If 2-points of transient recording technique is directly applied through PC clock then PC can not record transient correctly. It is because 70% sources of internal clock are used to record 2-points of transient and remaining 30% sources of clock are not enough for PC to perform its personal tasks. PC records data on certain buadrate. If data is not recording on certain buadrate then signal-to-noise ratio is low. Output of capacitance meter does not match with any standard buadrate of PC. Hence PC records data asymmetrically. This problem can be solved by the application of ADC. Whole transient is recorded for applied pulse then 2-points of maximum and minimum are sorted out. If two transients are recorded for pulse of same parameters are asymmetric. It is due to buadrate mismatching problem. There are other techniques which can be applied. Digital signal process (DSP), and programming of microcontroller chip.

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Glossary

A

Acceptor handshake: Listeners use this GPIB interface function to receive data, and all devices use it to receive commands.

Access board: The GPIB board that controls and communicates with the devices on the bus that are attached to it.

ADC: Analog to digital converter.

ANSI: American National Standards Institute.

ASCII: American Standard Code for Information Interchange.

Asynchronous: An action or event that occurs at an unpredictable time with respect to the execution of a program.

Automatic serial polling: A feature of the NI-488.2 software in which serial polls (autopolling) are executed automatically by the driver whenever a device asserts the GPIB SRQ line.

B

base I/O address: Input / output addresses.

BIOS: Basic Input/Output System.

board-level function: A rudimentary function that performs a single operation.

C

CFE Configuration: Enable is the GPIB command which precedes CFGn and is used to place devices into their configuration mode.

CFGn: These GPIB commands (CFG1 through CFG15) follow CFE and are used to configure all devices for the number of meters of cable in the system so that HS488 transfers occur without errors.

CIC : Controller-In-Charge The device that manages the GPIB by sending interface (CIC) messages to other devices.

CPU: Central processing unit.

D

DAC: Digital to analog converter.

DAV: (Data Valid) One of the three GPIB handshake lines. See *handshake*.

DCL: Device Clear is the GPIB command used to reset the device or internal functions of all devices.

Device-level function: A function that combines several rudimentary board operations into one function so that the user does not have to be concerned with bus management or other GPIB protocol matters.

DIO1 through DIO8: The GPIB lines that are used to transmit command or data bytes from one device to another.

DLL: Dynamic link library.

DMA: High-speed data transfer between the GPIB (direct memory access) board and memory that is not handled directly by the CPU.

Driver: Device driver software installed within the operating system.

E

END or END message: A message that signals the end of a data string. END is sent by asserting the GPIB End or Identify (EOI) line with the last data byte.

EOI: A GPIB line that is used to signal either the last byte of a data message (END) or the parallel poll Identify (IDY) message.

EOS or EOS byte: A 7- or 8-bit end-of-string character that is sent as the last byte of a data message.

EOT: End of transmission.

ESB: The Event Status bit is part of the IEEE 488.2-defined status byte which is received from a device responding to a serial poll.

G

GET Group: Execute Trigger is the GPIB command used to trigger a device or internal function of an addressed Listener.

GPIB: General Purpose Interface Bus is the common name for the communications interface system defined in ANSI/IEEE Standard 488.1-1987 and ANSI/IEEE Standard 488.2-1987.

GPIB address: The address of a device on the GPIB, composed of a primary address (MLA and MTA) and an optional secondary address (MSA). The GPIB board has both a GPIB address and an I/O address.

GPIB board: Refers to the National Instruments family of GPIB interface boards.

GTL: Go To Local is the GPIB command used to place an addressed Listener in local (front panel) control mode.

H

Handshake: The mechanism used to transfer bytes from the Source Handshake function of one device to the Acceptor Handshake function of another device. The three GPIB lines DAV, NRFD, and NDAC are used in an interlocked fashion to signal the phases of the transfer, so that bytes can be sent asynchronously (for example, without a clock) at the speed of the slowest device. For more information about handshaking, refer to the ANSI/IEEE Standard 488.1

hex Hexadecimal: A number represented in base 16, for example decimal 16 = hex 10.

I

ibcnt: (ib stands for interface board or device. ib is predirector of the statement for compiler so it is written before of each mnemonic) After each NI-488.2 I/O function, this global variable contains the actual number of bytes transmitted.

iberr: A global variable that contains the specific error code associated with a function call that failed. See Table1.

ibsta: At the end of each function call, this global variable (status word) contains status information.

ibclr: At the end of each command , this variable clear the device.

ibwrt: This Mnemonic is used to write the device.

ibrd: This Mnemonic is used to read the data from the device.

ibtrg: This Mnemonic is used to trigger the device.

ibrsp: This Mnemonic is used to check the response of the device.

ibwait: This Mnemonic is used to wait the device.

IEEE: Institute of Electrical and Electronic Engineers.

Interface message: A broadcast message sent from the Controller to all devices and used to manage the GPIB.

I/O (Input/Output): In the context of this manual, the transmission of commands or messages between the computer via the GPIB board and other devices on the GPIB.

I/O address: The address of the GPIB board from the point of view of the CPU, as opposed to the GPIB address of the GPIB board. Also called port address or board address.

ist: An Individual Status bit of the status byte used in the Parallel Poll Configure function.

K

KB: Kilobytes.

L

LAD (Listen Address) : language interface Code that enables an application program that uses NI-488 functions or NI-488.2 routines to access the driver.

Listener: A GPIB device that receives data messages from a Talker.

M

MAV: The Message Available bit is part of the IEEE 488.2-defined status byte which is received from a device responding to a serial poll.

MB: Megabytes of memory.

memory-resident: Resident in RAM.

MLA: A GPIB command used to address a device to be (My Listen Address) a Listener. It can be any one of the 31 primary addresses. MSA My Secondary Address is the GPIB command used to address (My Secondary Address) a device to be a Listener or a Talker when extended (two byte) addressing is used. The complete address is a MLA or MTA address followed by an MSA address. There are 31 secondary addresses for a total of 961 distinct listen or talk addresses for devices.

MTA (My Talk Address): A GPIB command used to address a device to be a Talker. It can be any one of the 31 primary addresses.

Multitasking: The concurrent processing of more than one program or task.

N

NDAC: (Not Data Accepted) One of the three GPIB handshake lines. See *handshake.*

NRFD: (Not Ready For Data) One of the three GPIB handshake lines. See *handshake.*

P

Parallel poll: The process of polling all configured devices at once and reading a composite poll response. See *serial poll* .

PIO: See *programmed I/O.*

PPC: Parallel Poll Configure is the GPIB command (Parallel Poll Configure) used to configure an addressed Listener to participate in polls.

PPD: Parallel Poll Disable is the GPIB command used (Parallel Poll Disable) to disable a configured device from participating in polls.

PPE: Parallel Poll Enable is the GPIB command used (Parallel Poll Enable) to enable a configured device to participate in polls and to assign a DIO response line. There

PPU: Parallel Poll Unconfigure is the GPIB command (Parallel Poll used to disable any device from participating in Unconfigure) polls.

Programmed I/O: Low-speed data transfer between the GPIB board and memory in which the CPU moves each data byte according to program instructions.

R

RAM: Random-access memory.

Resynchronize: The NI-488.2 software and the user application must resynchronize after asynchronous I/O operations have completed.

RQS: Request Service.

S

SDC: Selected Device Clear is the GPIB command used to reset internal or device functions of an addressed Listener.

Serial poll: The process of polling and reading the status byte of one device at a time.

Service Request See *SRQ*.

Source handshake: The GPIB interface function that transmits data and commands. Talkers use this function to send data, and the Controller uses it to send commands. See *acceptor handshake* and *handshake*.

SPD: Serial Poll Disable is the GPIB command used to (Serial Poll Disable) cancel an SPE command.

SPE: Serial Poll Enable is the GPIB command used to (Serial Poll Enable) enable a specific device to be polled. That device must also be addressed to talk. See *SPD*.

SRQ (Service Request): The GPIB line that a device asserts to notify the CIC that the device needs servicing.

Status byte: The IEEE 488.2-defined data byte sent by a device when it is serially polled.

Status word See *ibsta*. Table 2.

Synchronous: Refers to the relationship between the NI-488.2 driver functions and a process when executing driver functions is predictable; the process is blocked until the driver completes the function.

System Controller: The single designated Controller that can assert control (become CIC of the GPIB) by sending the Interface Clear (IFC) message. Other devices can become CIC only by having control passed to them.

T

TAD (Talk Address): See *MTA*.

Talker: A GPIB device that sends data messages to Listeners.

TCT: Take Control is the GPIB command used to pass control of the bus from the current Controller to an addressed Talker.

Timeout: A feature of the NI-488.2 driver that prevents I/O functions from hanging indefinitely when there is a problem on the GPIB.

TLC: An integrated circuit that implements most of the GPIB Talker, Listener, and Controller functions in hardware.

U

Ud (unit descriptor): A variable name and first argument of each function call that contains the unit descriptor of the GPIB interface board or other GPIB device that is the object of the function.

UNL: Unlisten is the GPIB command used to unaddress any active Listeners.

UNT: Untalk is the GPIB command used to unaddress an active Talker.

Table 1 Error Mnemonic

Error Mnemonic	iberr Value	Meaning
EDVR	0	Windows error
ECIC	1	Function requires GPIB board to be CIC
ENOL	2	No Listeners on the GPIB
EADR	3	GPIB board not addressed correctly
EARG	4	Invalid argument to function call
ESAC	5	GPIB board not System Controller as required
EABO	6	I/O operation aborted (timeout)
ENEB	7	Nonexistent GPIB board
EDMA	8	DMA error
EOIP	10	Asynchronous I/O in progress
ECAP	11	No capability for operation
EFSO	12	File system error
EBUS	14	GPIB bus error
ESTB	15	Serial poll status byte queue overflow
ESRQ	16	SRQ stuck in ON position
ETAB	20	Table problem

Table 2 Status Word Layout

Mnemonic	Bit Pos.	Hex Value	Type	Description
ERR	15	8000	dev, brd	GPIB error
TIMO	14	4000	dev, brd	Time limit exceeded
END	13	2000	dev, brd	END or EOS detected
SRQI	12	1000	brd	SRQ interrupt received
RQS	11	800	dev	Device requesting service
SPOLL	10	400	brd	Board has been serial polled by Controller
EVENT	9	200	brd	DCAS, DTAS, or IFC event has occurred
CMPL	8	100	dev, brd	I/O completed
LOK	7	80	brd	Lockout State
REM	6	40	brd	Remote State
CIC	5	20	brd	Controller-In-Charge
ATN	4	10	brd	Attention is asserted
TACS	3	8	brd	Talker
LACS	2	4	brd	Listener
DTAS	1	2	brd	Device Trigger State
DCAS	0	1	brd	Device Clear State