Capacitor-less LDO Design Techniques for Portable Applications in Nanometer CMOS

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Verily, in the creation of the heavens and the earth, and in the alternation of the night and the day, and in the ships (and vessels) which sail through the ocean carrying cargo profitable for the people, and in the (rain) water which Allah pours down from the sky, reviving therewith the earth to life after its death, and (the earth) in which He has scattered animals of all kinds, and in the changing wind directions, and in the clouds (that trail) between the sky and the earth, duty-bound certainly, (in these) are (many) signs for those who put their reason to work.

(Al-Baqarah : 164)

Dedicated to my parents .....

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Abstract

In the realm of modern electronics, effective power management is crucial, especially with the prevalence of System-on-Chip (SoC) technologies. Traditional Low-Dropout Voltage Regulators (LDOs) often rely on output capacitors, which can incur additional costs, increase board sizes, and expand pin counts. This study focuses on the development of two external capacitor-less Low-Dropout Voltage Regulator (LDO) designs in 55nm CMOS technology for portable applications. The first LDO design spans a voltage range of 1 to 4 V, maintaining a stable 1.2 V output across loads from 0.2 to 50 mA, with a power consumption of 1 mW only. Using a Transient Enhancement Circuit, It exhibits minimal voltage spikes (below 150 mV), a 0.1 us settling time, and a quiescent current of 59 μA under maximum load. The second LDO design integrates a slew rate enhancement circuit for improved transient responses. It remains stable throughout a 0–50 mA full load range without an output capacitor. The LDO's output voltage recovers within 0.4 μs with a voltage spike of less than 40 mV, demonstrating enhanced DC load control (0.031 mV/mA) consuming 71μW . It operates with a quiescent current of 22 μA and a 200 mV dropout voltage at 1V supply Voltage and regulate the circuit output Voltage at 0.8V. Both LDOs offer efficient load and line transient responses, reduced settling times, and resilience to process, voltage, and temperature variations, ensuring consistent and reliable performance.

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Abbreviations

V_{DD}	Supply Voltage
V_{DO}	Dropout Voltage
V_{FB}	Feedback Voltage
V_G	Gate Voltage
V_{in}	Input Supply Voltage
V_{DSAT}	Transistor's Saturation Voltage
V_{EA}	Error Amplifier Output Voltage
L_{HP}	Left Half Plane
R_{HP}	Right Half Plane
V_{out}	Output Voltage
V_{ref}	Voltage Reference
V_{SD}	Source-Drain Voltage
V_{SG}	Source-Gate Voltage
W	Channel Width of a Transistor
L	Channel Length of a Transistor
$\mu_{p/n}$	Transistor's Mobility
RF	Radio Frequency
β	Feedback Factor
Cgd	Gate-Drain Capacitance
C_L	Load Capacitor
C_M	Miller Capacitor
$CMOS$	Complementary Metal–Oxide–Semiconductor
CS	Common Source
C_{out}	Output Capacitance

Cox	Oxide Capacitance per Unit Area
DRC	Design Rule Check
EA	Error Amplifier
FoM	Figure of Merit
FVF	Flipped Voltage Follower
gm	Transistor's Transconductance
IC	Integrated Circuits
I_L	Load Current
I_Q	Quiescent Current
LDO	Low-Dropout
LNR	Line Regulation
LDR	Load Regulation

Chapter 1

Introduction

The demand for portable electronic gadgets is continuing to increase as our globe becomes more mobile. The increasing prevalence of long-lasting autonomous portable and wearable gadgets has led to a growing interest in the development of efficient power management units (PMUs). These PMUs are required to be miniaturized and have reduced power consumption in order to meet the demands of such technology[3]. The decrease in scale of semiconductor (MOS) transistors to nanometric dimensions presents several complex implications for physical properties and integrated circuit (IC) designs, specifically in the realm of analog IC designs.

The fundamental worry lies in the Gate Tunnelling Leakage Current (IGleak) as transistors become increasingly compact. This current has the potential to introduce a low-frequency pole (fgate), leading to a degradation in system stability, transient response time, and voltage fluctuations (V). In the past three decades, the importance of power management technology has increased due to the integration of tiny cellular phones, tablets, laptops, and wearable gadgets such as fitness trackers, smart jewelry, and implantable biomedical sensors into our daily lives. The Contemporary electronic devices have facilitated progress in various domains, including power conversion efficiency (PCE), reduction of dropout voltages, enhancement of operating speed, extension of battery life, and overall improvement in performance.

One of the fundamental design issues for portable electronic devices is to optimize power usage while ensuring reliable and effective power delivery.

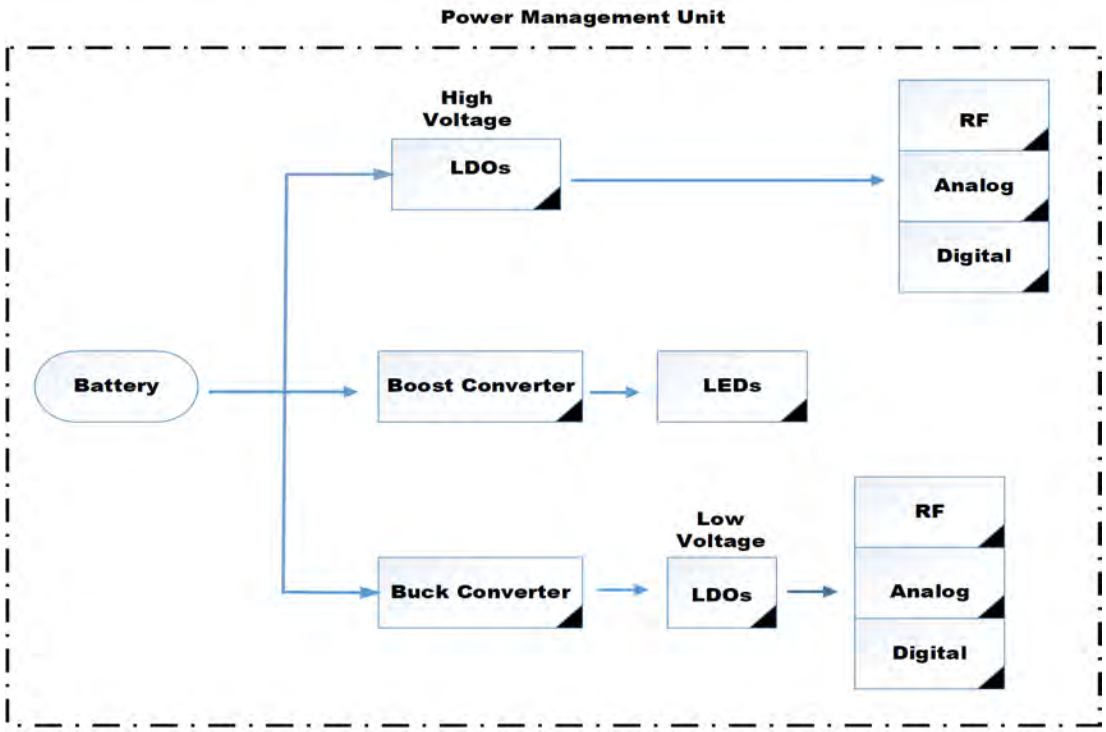


Figure 1.1: *Power management unit block*

In order to enhance the battery life of portable devices, the implementation of novel circuit designs is necessary inside power management systems. A power management unit comprises several components, including switching regulators such as buck converters, boost converters, and charge pumps, as well as linear regulators, predominantly low-dropout regulators (LDOs), and digital control logic as depicted in fig 1.1. To help minimize power consumption and extend battery life, the control logic allows transitioning between multiple voltage levels based on demand. Furthermore, it is important to note that the voltage of a battery diminishes gradually over a period of time. This is a challenge for circuits, as they require a consistent voltage in order to function at their highest efficiency. This is where the idea of capacitor-less LDOs comes into play to alleviate the issue.

This thesis centers on the development of an efficient power source for handheld devices, with the objective of achieving a System-on-Chip (SoC) solution that integrates the voltage regulator core and necessary supplementary circuitry into a single chip, thereby eliminating the need for external components. In this regard, CMOS technology implementation is the most cost-effective solution.

1.1 Power Management Unit (PMICs)

Every electronic device needs a power-source to work. Optimizing energy consumption and increasing device autonomy necessitates efficient battery management. A Power Management Unit (PMU) is responsible for managing the distribution of energy based on the real-time power supply requirement of certain circuits, including active, standby, sleep, and power-off modes.

Figure 1.2 depicts the three components that make up a PMU: a DC-DC converter, an analog LDO, and a digital LDO.

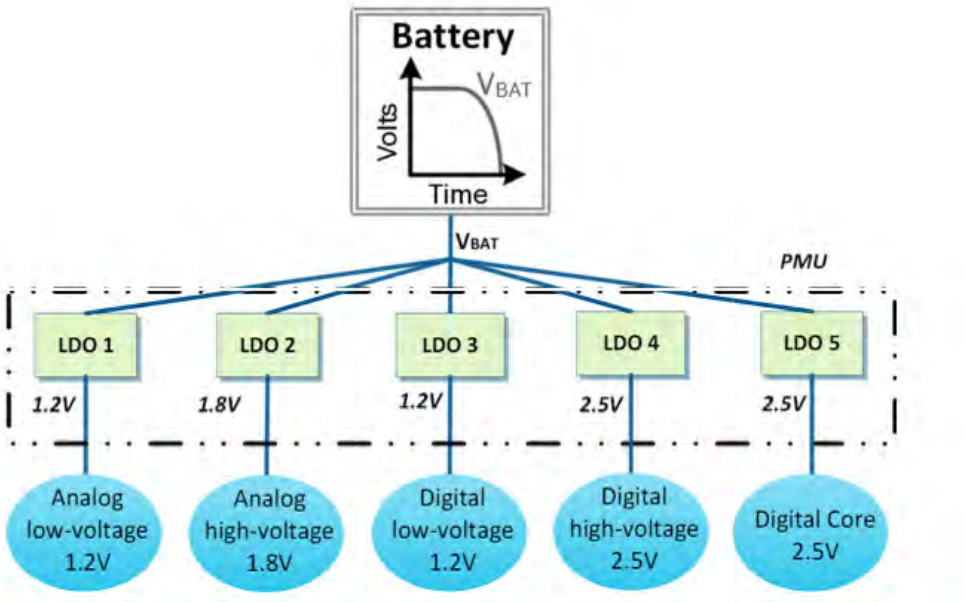


Figure 1.2: *Power management Unit with several LDOs (Low Dropout)*

The PMU is typically broken up into multiple parts based on the voltage levels that are required for specific blocks. Low noise and stable supply voltage are two of the most commonly desired requirements. The predominant components employed in power management are switching converters and linear regulators. Voltage regulators can be classified into two primary categories: linear regulators and switching regulators. Inductors and capacitors, which are utilized by switching regulators, take up a lot of circuit area.

These regulators use charge transfer to adjust voltage and are noisy owing to switching behavior. They usually convert high voltages to low voltages, although the output voltage can fluctuate and be noisy. In applications where energy transfer efficiency is critical, particularly in high voltage situations, switching regulators are typically used.

In this body of research, DC-DC converters, and more specifically LDOs, which are the components that are accountable for regulating voltage levels and guaranteeing a stable power supply, receive the majority of the attention.

1.1.1 Switching Regulators / DC-DC converter

Switching regulators serve the purpose for high load current or input-to-output differential voltages. These regulators exhibit quick switching behavior, toggling a series device between the on and off states. Another advantage over linear designs is that they can produce output voltages that are greater than or opposite to the input voltage. In contrast to linear regulators, these require additional parts, specifically a capacitor or inductor to store energy. A DC converter takes in a DC voltage at its input and transforms it to a different DC value at its output. A range of DC-DC converters exist, encompassing buck converters, boost converters, buck-boost converters, and flyback converters, among other types. Each category has unique properties and applications. Buck converters, for instance, take the input voltage and reduce it such that the output voltage is lower[4]. Boost converters, on the other hand, increase the input voltage to produce a greater output voltage. Buck-boost converters possess the capacity to perform both voltage step-up and step-down operations. The topology of the two converters is shown in Figure 1.3. One of the

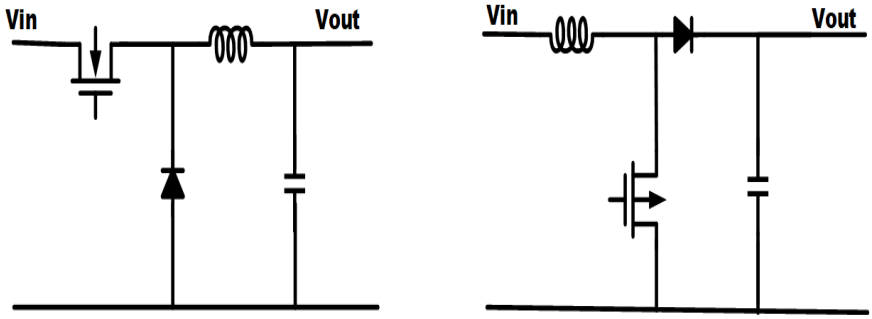


Figure 1.3: *Buck and Boost converter topologies*

primary concerns associated with the utilization of a DC-DC converter that is not exclusively designed for this purpose is the presence of ripple in the output voltage. To mitigate the effects of ripple and load fluctuations, an LDO (Low Dropout) regulator is employed subsequent to the DC-DC converter. The purpose of the DC-DC regulator is to reduce the voltage drop across the linear regulator under varying load situations, as depicted in Figure 1.4.

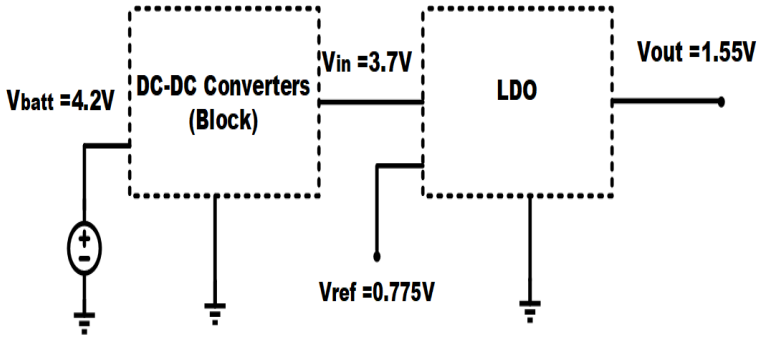


Figure 1.4: *Good linear efficiency regulation*

1.1.2 Linear Regulator

The linear regulator is a type of DC-DC voltage converter that operates by linearly regulating the DC voltage at the input to produce an output that has a decreased DC value (see Figure 1.5). The linear regulation of the output voltage confers a number of benefits, including improved power supply rejection, reduced output noise, and enhanced dynamic response, amongst others. The

primary limitations of this approach include sub-optimal efficiency and a constraint on the ability to perform down conversion. Variations in the DC input voltage have a significant impact on the power efficiency of linear regulators. This is because power efficiency is inversely related to the drop in voltage that occurs across the control device. The efficiency of a regulator decreases as the gap between input and output widens. Moreover, the magnitude of power loss worsens in direct proportion to the current load. Hence, in certain systems, the linear regulator might not be an appropriate choice due to its inability to handle high current loads. Two primary categories of linear regulators exist:

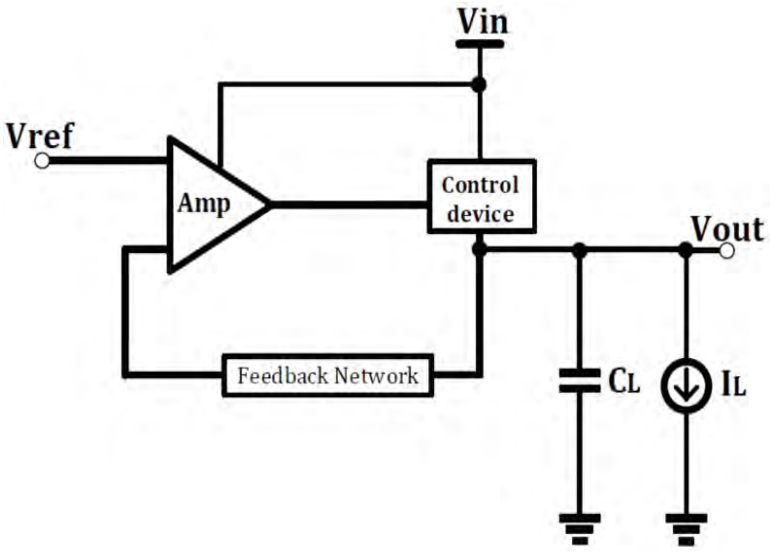


Figure 1.5: *Linear Regulator*

- Conventional linear regulators
- LDO regulators

The sole distinction between the two preceding architectures lies in the placement of a power transistor. A conventional linear regulator makes use of a transistor that is connected to the common drain. Alternatively, this transistor can be substituted with a BJT transistor or two transistors configured in a Darlington arrangement. There is a general relationship between the orientation of a power transistor and the mode of operation as well as the stability of the linear regulator.

1.1.3 Comparison

In the framework of portable devices powered by batteries, the linear regulator is commonly employed because to its advantageous characteristics, including simplicity, compactness, and cost-effectiveness. When the controlled voltage is lower than the supply voltage, linear regulators are often the best way to regulate power because they are inexpensive, easy to build, and small. These types of regulators are most suitable in situations where there is a need for minimal output noise, as well as a rapid reaction to both input and output disturbances. Low-power versions are cheaper and take up less chip space. In spite of the fact that switching regulators bring in a lot of limelight due to the great efficiency they offer, linear voltage regulators deliver the best solution for powering the circuitry in the majority of applications that include portable devices.

Table 1.1: Linear regulators vs. Switching regulators: a comparison

Regulator Type	**Linear**	**Switching**
Function	Only steps down	Steps up, steps down or inverts
Efficiency	Low to medium	High
External Components	No	Yes
Ripple/noise	Low	Medium to high
Design Complexity	Low	Medium to high
Total cost	Low	Medium to high
Waste heat	High	Low
Size	Small to medium	Medium to high

1.1.4 Low Drop Out (LDO) Regulator

The LDO (low-dropout) system is a common example of a negative feedback mechanism utilized to generate a stable and consistent output voltage, as depicted in Figure 1.6. As the output voltage increases, the operational amplifier (op amp) amplifies the voltage differential, resulting in an increase in the voltage across the gate of the pass element. The pass element is designed to limit the current supplied to the output, resulting in a decrease in the output voltage in order to maintain a consistent level of output voltage. The adoption of the feedback loop in the system enhances the precision and resilience of the output voltage of the low-dropout regulator (LDO) in the presence of load and line transients. Due to the inherent noise present in the voltage output of switching regulators, the utilization of low-dropout regulators (LDOs) becomes necessary in order to ensure a stable and clean voltage supply. This requirement is complemented by the need for the LDO to operate with minimal power consumption and exhibit a relatively low dropout value.

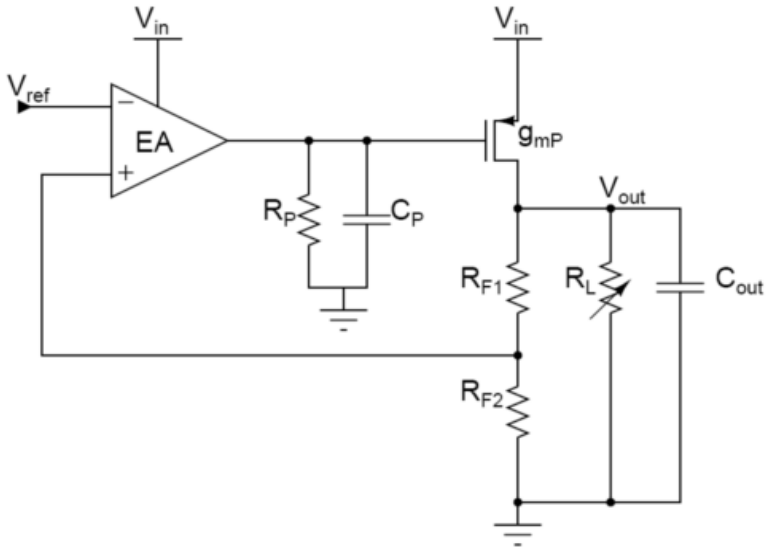


Figure 1.6: *LDO regulator (low dropout)*

The mode of operation of the regulator is determined by the dropout voltage across the power mosfet. The operation of a linear regulator can be categorized into three distinct regions: the linear region, the dropout region, and

the off-region. The two operational states and their related input voltage are depicted in Figure 1.7, which showcases the usual input-output voltage specifications of a linear regulator. The importance of low-dropout (LDO) voltage

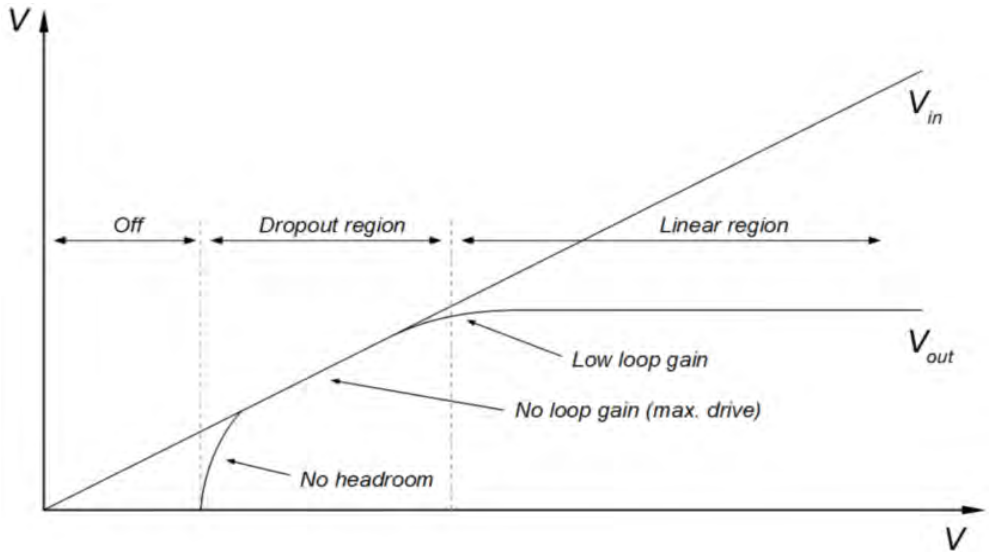


Figure 1.7: *LDO voltage regulator input-output voltage characteristics*

regulators resides in their capacity to effectively tackle the difficulties linked to voltage regulation across diverse applications. In contrast to alternative voltage regulators, including switching regulators, low-dropout regulators (LDOs) function in a linear mode. This renders them useful to use in applications where the reduction of noise and switching glitches is imperative, like in analog and low-power devices. These devices belong to a category of linear voltage regulators that exhibit enhanced power efficiency. The enhancement in efficiency in comparison to traditional linear regulators is achieved through the substitution of the common-drain pass element with a common-source pass element, resulting in a reduction of the minimum voltage drop necessary across the control device [5]. The basic objective when using a low-dropout regulator (LDO) is to sustain a consistent output voltage, often characterized by a minimal dropout voltage. The term "dropout voltage" pertains to the minimal voltage gap between the input and output of a low-dropout regulator (LDO), at which point the LDO's ability to efficiently regulate the output voltage is

compromised.

$$V_{drop} = V_{in} - V_{out} \tag{1.1}$$

Low dropout voltage (LDV) is a key characteristic of low dropout regulators (LDOs), enabling them to deliver regulated output voltages that closely approximate the input value, although the input voltage is only marginally higher than the intended output voltage. These types of circuits are well-suited for a wide range of applications, especially in the context of handheld devices. This is primarily due to their minimal voltage drop (Vin-Vout), as well as their beneficial properties such as low noise levels, compact size, and simplified design. They are valued for low-power uses, primarily owing to their enhanced efficiency as well as their comparatively reduced cost and reduced quiescent current. LDOs shine in portable electronics, which face challenges in size, power efficiency, and battery life. Because of their small form factor, low power consumption, and tolerance for minor voltage differentials, they find widespread use in portable electronic gadgets. Power-hungry components like memory chips, microprocessors, and sensors can function at their highest efficiency with the help of linear regulators.

1.2 Fundamental Structure/Design Elements

The basic components of an LDO regulator are:

- Error Amplifier
- Pass Transistor
- Reference Voltage
- Network Resistive Feedback

1.2.1 Error Amplifier:

The error amplifier constitutes one of among the most crucial components of the LDO regulator's design. By comparing the input voltage levels and ma-

nipulating the gate voltage of the power mosfet accordingly, it maintains regulation. Typically, an operational amplifier with up to three phases is employed to achieve a high Gain. For the sake of LDO stability over a variety of loads, the error amplifier need to implement a sort of compensation. Plus directly affecting the transient activity of the LDO is the bandwidth. A decent operational amplifier should also have a low bias current, a low offset, and a high DC gain.

1.2.2 Pass Transistor

The primary factors pertaining to the pass transistor in a low-dropout (LDO) voltage regulator are its maximum current capacity, dropout voltage, and power usage. Several studies conducted by researchers [6, 7] have demonstrated that voltage regulators employing NMOS transistors as pass devices exhibit certain characteristics. Despite the advantage of requiring less area for an equal drain current owing to greater mobility, these regulators have a higher dropout voltage requirement to maintain the transistor in the saturation region compared to PMOS transistors. Consequently, the supply voltage must be considerably greater than the voltage at output. According to reference [8], it is possible to decrease the dropout voltage across an NMOS transistor by raising its gate voltage beyond that of the supply. However, certain configurations of NMOS pass devices require the inclusion of a charge pump circuit to enhance the headroom of the NMOS pass transistor for this purpose. The dropout voltage also has major implications in determining the pass device's power consumption. Being a pass transistor, the PMOS uses quiescent current at a lower value than the NMOS since the former has a lower dropout voltage [10]. With this in mind, the LDO voltage regulator's pass device is a PMOS transistor, which allows for a low dropout voltage to be achieved. The schematic for a pass transistor can be seen in Figure 1.8. The load current is regulated by the pass transistor. The error amplifier regulates its gate. In most cases, pass transistors will have a tremendously large footprint. To achieve a low dropout voltage, this is done to lower the on resistance (discussed more in this write-up). Whereas bigger transistors take up more room, leaving less

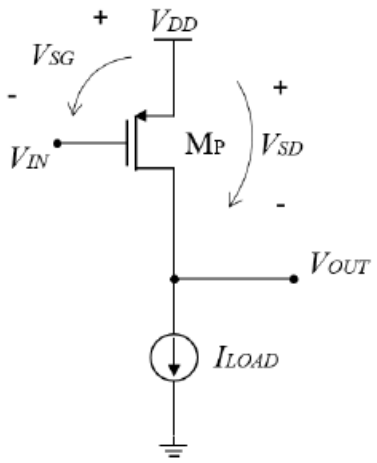


Figure 1.8: *Pass Transistor design*

room for other circuitry. In IC designs, where minimalism and effective space usage are paramount, this might be a cause of worry here. Higher parasitic capacitance and resistance might reduce the LDO's efficiency if the transistors are too large. Consequently, despite bigger transistors may provide certain output benefits, there may be compromises when it comes to area usage, cost, and possible performance constraints due to their larger size.

1.2.3 Reference Voltage

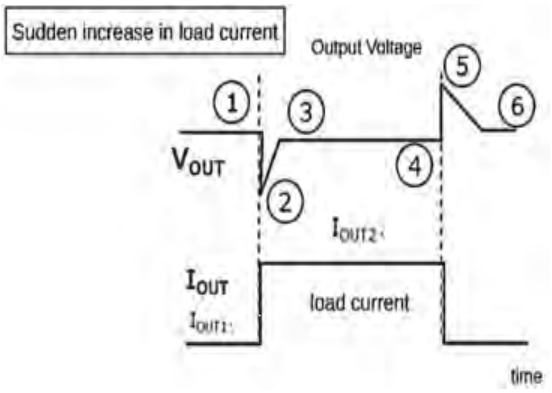
The voltage reference is an essential component in the error amplifier of a low-dropout (LDO) regulator, as it is responsible for measuring its output voltage and ensuring proper regulation. Voltage references are commonly produced through the utilization of bandgap circuits, which benefit from the complementary characteristics of semiconductor materials to yield a relatively stable voltage output, even in the presence of temperature fluctuations. Nevertheless, the present study did not incorporate or develop a bandgap circuit; instead, a fixed direct current (DC) source was employed as a point of reference.

1.2.4 Resistive Feedback Network

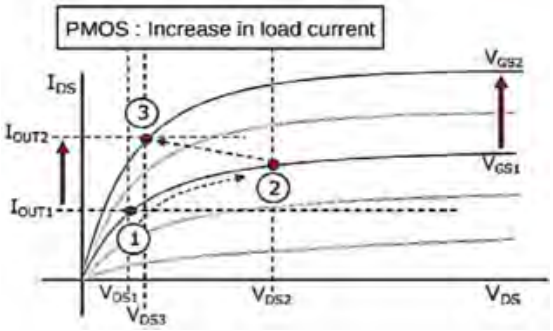
Typically, the output of a resistive divider network consists of two resistors wired in series. The output voltage is effectively level-shifted, and the resulting voltage is used as a reference for the error amplifier's inputs. The feedback factor has an immediate and decisive impact on the loop gain; hence, a value that is greater is preferred for improved power supply noise rejection. Whenever each of the two resistors has the same value, the most common feedback factor used in design is 0.5.

1.3 Operation

It is imperative that the output voltage remains consistently steady in relation to fluctuations in both the load and the power supply. Once the load is activated, a negative feedback loop modifies the gate voltage of the pass transistor, allowing it to supply the current to the load.[9], [10] Likewise to this, the pass transistor enters the cutoff (subthreshold) zone and consumes barely any current to maintain regulated output voltage when the load is turned OFF, as depicted in Figure 1.9(a). At first, as depicted in Figures 1.9(b) and 1.9(c), A biasing is applied to the output voltage at the -1 position. The output voltage shifts from position 1 to 2 to deliver the load current (Vsd will go up by reducing Vd) until the loop begins addressing to the sudden increase in load current I_{OUT1}. After the loop noticed and reacted to the output voltage, it returns to position-3. Because of the different values for the bias current, the output voltage will see a marginal drop as a result. The phenomenon being described here is referred to as load regulation. [11]. As in Figure 1.9 (b) and Figure 1.9(c), we sustain the beginning of the output voltage at position 4. In the event that there is an abrupt surge in load current from I_{OUT1} to I_{OUT2} , the voltage will undergo a shift from position-4 to position-5 in order to sustain the output current change before the loop responds. [11] As soon as the loop registers a response, the output voltage will change from position 5 to position 6. In addition to that, the output voltage that is produced varies slightly from one instance to the next.



(a)



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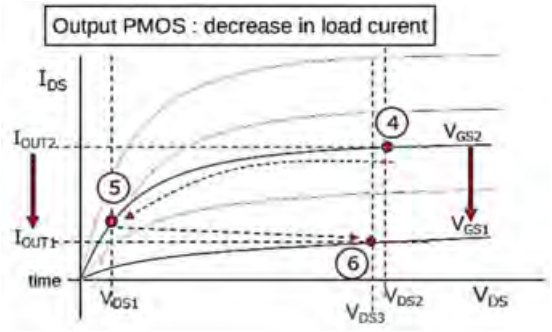

(c)

Figure 1.9: *(a), (b), (c) in LDO working*

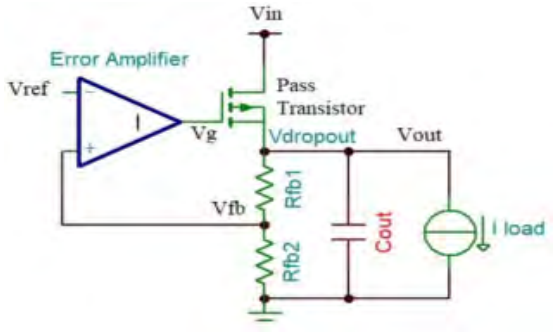

Figure 1.10: *PMOS based LDO*

1.4 LDO Linear Regulator Characterization

The conventional method for characterizing an LDO involves running simulations, taking bench measurements, and putting the results through validation procedures. This aids in making whether the LDO is fit for its intended purpose in terms of features, efficiency, and resiliency. There are three primary kinds of voltage regulator specifications: static (or steady-state), dynamic (or transitional), and high-frequency. [12].

1.4.1 Static-state Specifications

The impacts of the line and load regulation, plus temperature coefficients are all considered to be static-state parameters. Each of the DC or steady-state requirements may be found in Figure 1.11, which serves as a point of reference.

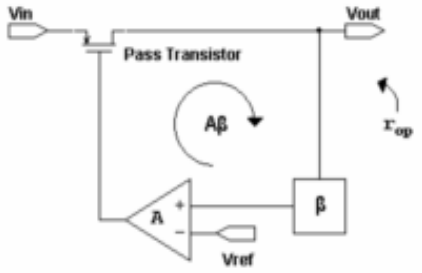

Figure 1.11: *Closed Loop system*

Line regulation Line regulation is a measure of the ability of a low-dropout (LDO) regulator to efficiently keep a constant output voltage in the presence

of fluctuations in the input voltage. The metric of line regulation involves changing the input voltage while simultaneously observing the output voltage across all corresponding variations. Regardless of whether the input voltage goes upward or downward, the low-dropout regulator (LDO) remains steady, ensuring an uninterrupted, constant output voltage to supply power to sensitive devices. The desired line regulation might be zero, indicating that the output voltage remains uninfluenced by variations in the input voltage.

Equation 1.2 provides an expanded equation for line regulation.

$$\frac{\Delta V_{\text{out}}}{\Delta V_{\text{in}}} = \frac{g_{mp} r_{op}}{A\beta} + (\frac{1}{\beta})(\frac{\Delta V_{\text{REF}}}{\Delta V_{\text{in}}}) \tag{1.2}$$

When provided with a desirable quality input voltage reference, some factors that are influenced are the loop gain, Aβ, and the gain of the pass device, gmprop. The line regulation can be approximated as the quotient of the gain of the pass device and the gain of the loop. In order to enhance the line regulation, it is vital for the low-dropout (LDO) regulator to possess a loop gain of significant magnitude. The clarification of these quantities is evident inside discussions on LDO regulator architecture.

Load regulation: Variation in output voltage due to varying load current for a given input voltage is what this term describes. By changing the load current and watching the output voltage, we can gauge the accuracy of the load regulation. The load regulation is influenced by the loop gain, Aβ, and the output impedance of the pass transistor, rop. The aforementioned relationship is presented in equation 1.3.

$$Loadreg = \frac{\Delta V_{out}}{\Delta I_{out}} = \frac{r_{op}}{1 + A\beta} \tag{1.3}$$

In the hypothetical scenario when the open-loop gain of the low-dropout regulator (LDO) is considered infinite, it can be inferred that the load regulation would approach a value close to zero. Furthermore, it should be noted that the load regulation is enhanced as the output impedance of the pass device decreases. By reducing the output resistance and enhancing the open-loop gain, the circuit may efficiently mitigate fluctuations in the input voltage, leading

to enhanced load management. Given the inherent lack of control over the output impedance of the pass device, it is preferable to setup loop gain with significant order to provide optimal load regulation.

Temperature Dependence: Variations in temperature might lead to a deviation in the reference voltage away from the optimum level. The thermal stability and resilience of the circuit are assessed by evaluating its behavior under various temperature environments. The process of temperature assessment involves subjecting the design to several temperature conditions and examining its output voltage, voltage drop, and other significant measures. Equation 1.4 provides the temperature coefficient.

$$T_C = (\frac{1}{V_{out}}).(\frac{\alpha V_{out}}{\alpha T_{emp}}) \tag{1.4}$$

$$T_C = (\frac{1}{V_{out}}).(\frac{\Delta V_{TC}}{\Delta T_{emp}}) \tag{1.5}$$

$$T_C = (\frac{\Delta VTC_{ref} + \Delta VTC_{vos}}{V_{out}.\Delta T_{emp}}).(\frac{V_{out}}{V_{ref}}) \tag{1.6}$$

Both the highest current and the lowest possible battery voltage are set by the dropout voltage of an LDO regulator. The requirements namely dropout voltage, highest load current, and lowest battery voltage, are based upon the pass transistor conditions. In a specific low-dropout (LDO) design, it is standard to define the highest load current and the lowest supply voltage that the system can withstand while ensuring the pass transistor remains in a state of saturation. Equation 1.5 establishes a correlation between the dropout voltage of a low-dropout (LDO) regulator and the various parameters associated with the device. In this equation, I_{LOAD} represents the highest current flow at the output that the device can tolerate without compromising its functionality.

$$V_{dropout} = I_{LOAD}.R_{ON} = V_{DSAT.PMOS} \tag{1.7}$$

An increase in the source-gate voltage (VSG) and/or a larger W/L aspect ratio will reduce the $R_{DS.ON}$ of the pass device. Because the power rails that connect

to the integrated circuit in real circuits are VIN and ground, the gate voltage can never be lower than ground. This suggests that VIN is the upper limit for VSG. The channel width is determined by the designer, whereas the channel length is determined by the lowest channel length determined by the process technology. Since the die area constraint determines the width, the pass device is typically as large as possible within that width. The ability to pull the gate as close to the ground as you can is the primary obstacle that must be overcome in order to successfully reduce the R_{DSON}.

The physical dimensions of the pass device, the dropout voltage, and the power consumption limitations tend to be dictated by the highest allowable load current. In order to be able to deal with the additional parasitic capacitances that come as a result of higher device sizing, the highest current load specification has to be improved, which in turn causes the overall wafer size of the pass device and the control circuitry to rise. Additionally, the ground pin current must increase. Determining the parameters for meeting area and ground pin current can pose challenges, particularly when dealing with a substantial high load current.

1.4.2 Dynamic-state Specifications:

Different from steady-state specifications, dynamic-state specifications rely on the characteristics of the large signal LDO regulator. The dynamic state performance of an LDO depends on the charging and discharging of the gate capacitance. It has an immediate impact on the LDO's sensitivity to load and line transients, start-up and shutdown behavior, and dynamic stability. When the load current is switched from lowest to highest or vice versa, the LDO's output voltage either undershoots or overshoots. The worst-case load current fluctuation is shown in Fig. 1.12, where the load current abruptly changes from its maximum to its minimum value, and back again.

The variation of output voltage can be represented mathematically as (1.8).

$$\Delta V_{out} = \frac{I_{out}.\Delta t}{C_{out}} \tag{1.8}$$

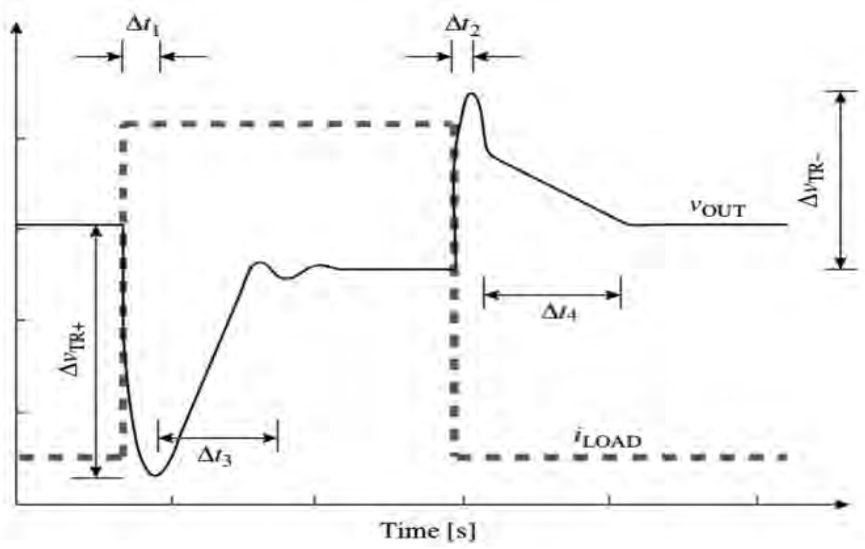

Figure 1.12: *Typical transient reaction to sudden load current changes*

The regulator's ability to effectively address rapid current load changes is based upon several factors, including the load current, the output capacitor, and the settling time of the low-dropout (LDO) regulator.
The response time Δt to these transient glitches is stated by the equation (1.9), and it can be accelerated by increasing the output capacitance C_{out}. And a larger BW_{CL}, denoting a larger quiescent current. Thus, unlike traditional LDOs, output capacitor-less LDOs exhibit bad load transients. The open loop phase margin and Δt determine what time it takes for the output voltage to stabilize during load transients. To calculate the loop response time Δt, we add the slew rate time t_{SR} to the inverse of the LDO's closed-loop bandwidth BW_{CL}.

$$\Delta t \approx \frac{1}{BW_{CL}} + t_{SR} \tag{1.9}$$

$$t_{SR} = \frac{C_P.\Delta V_P}{I_{SR}} \tag{1.10}$$

Pass transistors are typically intended to have a low dropout voltage, resulting in a reduced V_{Dsat} at maximal current. Consequently, these transistors tend to have larger physical dimensions, leading to the presence of significant

parasitic capacitance (Cp) at their gate. The process of either turning on or off the pass transistor requires the charging or discharging of the gate capacitance. The time frame of this process has a direct impact on the rate at which the pass transistor may react to alterations. An increased gate capacitance will necessitate more time for charging or discharging, hence leading a reduced slew rate. The gain-bandwidth product is a parameter that signifies the highest possible frequency at which a circuit can efficiently amplify signals. When the slew rate surpasses the gain-bandwidth product (GBW), it means that the transistor's speed of switching is comparatively higher in relation to the amplification capabilities of the circuit.

In the given situation, the pass transistor exhibits a prompt response to instantaneous variations in the load current, hence facilitating a timely and precise adjustment of the output voltage. The reduced response time contributes to the mitigation of notable transient voltage spikes at the output voltage node while experiencing rapid load transients.The optimization of gate capacitance management plays a crucial role in enhancing the dynamic performance and ensuring stable voltage regulation in the low-dropout regulator (LDO) system. It is imperative to ensure the appropriate sizing and design of the pass transistor, as well as the corresponding circuitry, including the gate driver and biasing network.

1.4.3 High Frequency Specifications:

A low-dropout regulator's (LDO) operation is heavily influenced by its high-frequency parameters, especially the power supply rejection ratio (PSRR) and noise characteristics. The PSRR and noise spotted at frequencies above the gain-bandwidth product are often specified by LDO regulators. [12]. The Power Supply Rejection Ratio (PSRR) quantifies the LDO's capacity to attenuate variations in the input power supply voltage. A regulator with a high Power Supply Rejection Ratio (PSRR) demonstrates its ability to efficiently mitigate fluctuations in the input power source and maintain a consistent output voltage. The importance of this aspect becomes particularly significant in scenarios where variations in the input supply have the potential to influence

the output voltage. A high power supply rejection ratio (PSRR) is essential in order to guarantee an effective and constant voltage control. The error amplifier and pass transistor are integral components in enhancing the power supply rejection ratio (PSRR) of the regulator. The utilization of a high-gain error amplifier enables efficient amplification and mitigation of fluctuations in the input supply voltage, hence minimizing their influence on the output voltage. Moreover, the large bandwidth facilitates the rapid response of the error amplifier to variations in the input supply. The power supply rejection ratio (PSRR), commonly denoted as PSRR, is typically represented as a ratio and is mathematically defined in equation (1.11).

$$PSRR = 20log_{10}.\frac{V_{out,ripple}}{V_{in,ripple}} \tag{1.11}$$

The level of noise generated is mainly influenced by the transconductance of the input stage. It is noteworthy to mention that the subsequent stages of the low-dropout (LDO) regulator, such as amplifiers or buffers, generally do not make a major difference to the output noise. This phenomenon occurs because of the slightly reduced volume of noise generated during these phases in comparison to the noise injected during the very first input stage. The enhancement of transconductance, which refers to the relationship between the input voltage and the output current, can be achieved by increasing the size of the input transistors. Nevertheless, attaining the most favorable noise figure necessitates an in-depth study suited for every model. A simplified LDO design is presented in Fig 1.13.

Any voltage regulator's performance is crucial.The efficiency of an LDO (low dropout) regulator is measured via the ratio of its output power to its input power. It reveals how well the circuit regulates power throughout the transformation from the input voltage to the output voltage. The formula for determining efficiency is as follows:

Efficiency = (Output Power / Input Power) * 100

$$Efficiency = \frac{I_{load}.V_{out}}{I_{in}.V_{in}} \tag{1.12}$$

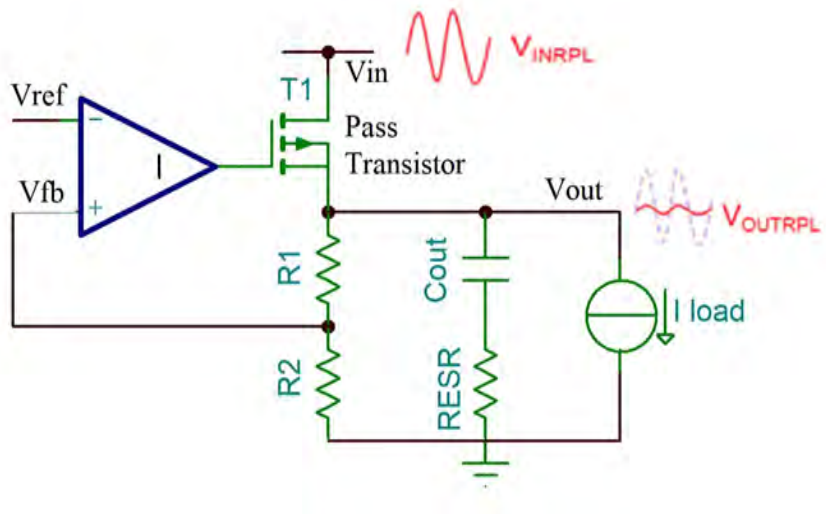

Figure 1.13: *A simple LDO architecture*

$$Efficiency = (\frac{I_{load}}{(I_{load} + I_Q)}).(\frac{V_{out}}{V_{in}}) \tag{1.13}$$

This varies with different loads, especially low and high current loads. The formula for light loads is as follows:

$$Eff = \frac{I_{load}}{I_{load} + I_Q} \tag{1.14}$$

An LDO often has a lower voltage conversion efficiency, which is the ratio of output to input. The low load-input power, the existence of quiescent current, and the effect of the dropout voltage are all contributing factors. A portion of the input power is not delivered to the load because of quiescent current, which involves the current consumed by the LDO itself. This means that some of the power going into the LDO is used for internal processes instead of going to the load. This makes the economy even worse when the load is small. To make up for this, LDOs with ultra-low quiescent currents are made for low-power uses and can work more efficiently.

Tradeoffs in Specifications Most of the requirements set by the LDO regulator are interconnected and result in substantial tradeoffs. Efficiency, transient response, and stability are the most important parameters. In the presence of

strict limitations, the optimization process quickly gets complicated. When developing the LDO regulator, the tradeoffs will become more clear.

1.5 Motivation and Objectives for Designing LDOs:

For devices to provide accurate voltage regulation, efficient power management, and consistently reliable performance, low-dropout regulators (LDOs) are a crucial part of today's electronic systems. Several factors influence both its design and implementation. Following that, LDOs regulate voltage, so their output voltage is stable as well as precise. This is very important for systems that require it. This is particularly paramount in contexts where strict voltage tolerances are required to prevent malfunctions or damage to the system. Power dissipation is reduced because of the low voltage drop between input and output that is a hallmark of LDOs. They meet the stringent power consumption of energy-conscious applications, battery-powered gadgets, and other systems setting up LDOs.

LDOs are also exceptional in their ability to reject noise, successfully filtering out high-frequency noise and ripple that may be found in the input power supply. This capacity to maintain a clean power supply is of utmost significance in several applications, such as audio amplifiers, data acquisition systems, and communication devices, in order to work accurately and reliably. In addition to this, they exhibit rapid transient response, meaning they can quickly adjust to varying loads and other types of transient circumstances. Even though the load is constantly shifting, this maintains a constant and well-regulated output voltage. Applications such as microprocessors, memory modules, and communication devices all benefit substantially from the quick transient response of LDOs since it enables reliable operation even while the load is changing dynamically.

Along with their strong efficiency features, low-dropout regulators (LDOs) also possess attributes such as small size and integration capabilities. These components are offered in compact packaging options and can be seamlessly integrated into application-specific integrated circuits (ASICs), system-on-chips (SoCs), and other types of integrated circuits. The compact size and integra-

tion of low-dropout regulators (LDOs) allow for the creation of space-efficient designs, making them well-suited for many applications such as portable devices, wearables, and miniature electronics. In general, the rationales underlying the design and implementation of low-dropout (LDO) regulators pertain to the requirements for accurate voltage control, effective power administration, noise mitigation, quick response to sudden changes, and compact integration within diverse electronic systems. Low dropout regulators (LDOs) have become prevalent in a diverse range of electronic systems and sectors. There are several noteworthy applications of low-dropout regulators (LDOs), which are as follows:

- Portable Electronics: In order to maintain a constant voltage and manage power efficiently in smartphones, tablets, portable media players, wearables, and more, LDOs are commonly used.
- Automotive Electronics: A vehicle's control unit, infotainment system, sensors, and other essential components rely on LDOs to supply them with stable, regulated power.
- Industrial and Automation Systems: In industrial automation, robotics, control, and instrumentation systems, LDOs are used to regulate voltage and filter out noise so that measurements and readings might get validated.
- Medical Devices: Patient monitoring, infusion pumps, diagnostic equipment, and implanted devices use LDOs to power sensitive electronics and ensure patient safety.
- Communications and Networking Equipment: A constant and controlled power supply is essential for the reliable transmission and networking of data, thus LDOs are utilized in telecommunications infrastructure, network switches, routers, and wireless access points.
- Aerospace and Defense Systems: For ensuring a steady and consistent power supply in harsh conditions, avionics systems, satellites, radar systems, and military equipment typically require LDOs.

- Consumer Electronics: Low dropout regulators (LDOs) are utilized in a diverse array of consumer electronic devices, including televisions, stereo systems, gaming consoles, cameras, and domestic appliances. These regulators serve the purpose of delivering regulated power to a multitude of components and subsystems within these devices.
- IoT (Internet of Things) Devices: LDOs are incorporated into Internet of Things devices such as sensors, smart home devices, and environmental monitoring systems to ensure a consistent and efficient power supply for dependable data sensing, processing, and communication. Examples of IoT devices include smart home gadgets.

The above instances only scratch the surface of the many fields in which LDOs find value. The requirement for precise voltage regulation, effective power management, and peak performance across a wide range of applications has made LDOs an indispensable part of today's electronic systems. Researchers have tried a wide range of strategies to boost productivity. Current boosting, slew boosting, and the Transconductance Boosting technique are only a few of the instances of these methods. Adaptive biasing and other enhancement circuits, such as those for increasing slew rate or smoothing out transients, are two more. The transient enhancement circuit aids in mitigating the effect of load variations, keeping voltage regulation precise and reducing output voltage swings. They expedite the LDO's ability to reach the predetermined output voltage by increasing the rate with which the voltage may rise or fall. Such modifications boost the LDO's overall performance by enhancing its transient response and output voltage regulation. Chapters 3 and 4 provide the results of an extensive study and design into transient enhancement circuit and slew rate enhancement circuit.

1.6 Thesis Organization

This thesis is organized into 5 chapters. Chapter 1 is a brief introduction to voltage regulators, their characteristics and system-level considerations. Chapter 2 provides stability Analysis and compensation, covers the state-of-the-

research, and a brief review of previous works. Chapter 3 introduces an LDO voltage regulator circuit with optimized undershoot and overshoot incorporating Transient Enhancement circuits and provide simulation results and layout. Chapter 4 illustrates another block/schematic level composition of the studied Low Dropout voltage regulator with slew rate Enhancement Technique in CADENCE, describing how each block is designed, and their performance and shows the simulation results and layout of the design. Finally, Chapter 5 presents the conclusion of this work.

Chapter 2

State-of-the-Art

The efficiency of most traditional low-dropout regulators (LDOs) is significantly impacted if the external capacitor is lowered by several orders of magnitude. The lack of a substantial external output capacitor poses many design issues in terms of both AC stability and load transient adaptability. Traditional low-dropout (LDO) regulators commonly employ a sizable external capacitor to establish the dominant pole and furnish an immediate charge source when faced with rapid load transients.

The big off-chip capacitor allows this conventional LDO to attain a good transient response, which is an additional benefit. Because this capacitor acts as a current path into the load during the fast load transient depicted in Fig. 2.2 before the gate of the pass element is modified via the slow path loop. The output capacitor serve as the fastest path, followed by the pass element and finally the load. The feedback loop and error amplifier are the slowest. The big output capacitor can supply the instantaneous load current need without waiting for the error amplifier's sinking or sourcing current to change the output voltage.

But the big capacitor off-chip takes up a lot of room and requires an external pin for the chip that needs a lot of space on the printed circuit board (PCB).So, an LDO without a capacitor needs an internal fast transient path to make up for the lack of a big external capacitor.Compensation may be categorized as either external or internal. Miller compensation is a method that is used a lot [1]. In this chapter, we revisit the fundamental capacitor-less LDO regulator

depicted in Figure 1 in order to accomplish the given goal.

2.1 AC Stability

Bode graphs study stability. By analyzing a circuit's open-loop gain and phase as a function of frequency, it is possible to ascertain whether or not the circuit is stable. Bode plot examination revealed gain and phase margin. Gain margin measures how much open-loop gain can be increased while maintaining stability. It is the difference between unity gain and amplifier gain at 180 phase frequency. The phase margin is the phase angle at unity gain frequency minus 180. The amplifier is stable only when phase margin is greater than 45.

LDO regulators employ a feedback mechanism in order to sustain a consistent output voltage, thereby making stability a consideration in the design process [13]. In order to prevent oscillation in feedback systems, it is necessary to satisfy Barkhausen's criteria [14]. It is imperative that the phase shift within the loop remain below 180 degrees when the loop gain surpasses unity. Figure 2.1 illustrates a general feedback system.

$$|KH(j\omega)| < 1 \tag{2.1}$$

$$\angle KH(j\omega) = -180^{\circ} \tag{2.2}$$

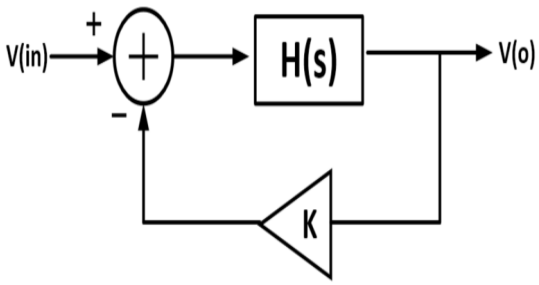

Figure 2.1: *Typical Feedback System*

2.2 Frequency compensation

Operational amplifiers exhibiting single-pole characteristics in the frequency domain are inherently stable due to the fact that their phase margin consistently remains at or above 90 degrees. In the context of multi-pole amplifiers, the potential for decreased stability and eventual instability of the amplifier arises. Hence, various techniques exist to alter the open-loop transfer function for the purpose of achieving stability in the amplifier, a process commonly referred to as frequency compensation.

2.3 External Compensation

The easiest way for compensating an LDO regulator in classical architecture is to use a large capacitor (about µF) at the output node. Figure 2.2 shows the topology again for convenience.

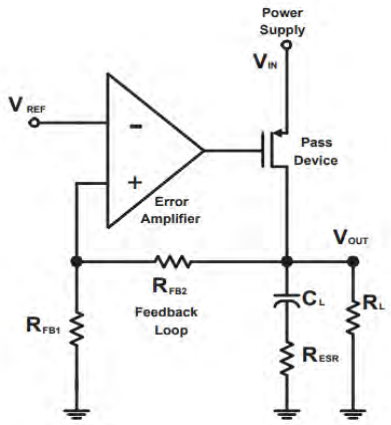

Figure 2.2: *Schematic of LDO with unity gain feedback: : without body bias control*

When it comes to frequency correction, using an external capacitor is highly useful. Only in situations when PCB area utilization is not a concern may external compensation be used practically and effectively. Meanwhile, modern studies are concentrating on finding ways to eliminate the external capacitor without sacrificing reliability, speed, or PSR performance. Here are some pros

and cons of using external compensation:
Advantages

- This method of compensating an LDO regulator offers the easiest and most flexible option.
- The error amplifier, pass transistor, and feedback network current parameters are all that are needed to calculate the voltage regulator's quiescent current (IQ).
- The whole of the load current range is covered with guaranteed stability.

Disadvantages

- When connecting the compensation capacitor over the board (PCB area consumption), an external pin is needed.
- It cannot be built into extremely compact and light-weight portable devices like cell phones, WSN sensors, GPS units, and so on.
- There is no way to precisely predict the rESR value because both it and the capacitor's properties vary with frequency. This has the potential to alter both the AC response and the transient response.The utilization of external compensation for LDO voltage regulators has been extensively documented in the literature [9–13]. However, a limitation persists in terms of system-on-a-chip (SoC) integration, as the inclusion of the external capacitor remains a challenge due to the inability to integrate it alongside the entire low-dropout (LDO) circuitry. Furthermore, it should be noted that the rESR value exhibits variation based on the specific characteristics of the capacitor being considered.

2.4 Internal Compensation

The LDO regulators with internal compensation are commonly referred to as capacitor-less LDOs. Internal compensation enables the complete integration of the LDO regulator with other circuits within the system on chip (SoC). This

approach is neither reliant on a large capacitor at the output, nor is it dependent on the equivalent series resistance (rESR) of the capacitor. Furthermore, it enhances the transient response characteristics of the low-dropout (LDO) regulator. The primary objective of internal compensation is to eliminate the need for an external capacitor in the LDO regulator, hence achieving a fully-integrated solution while maintaining stability.

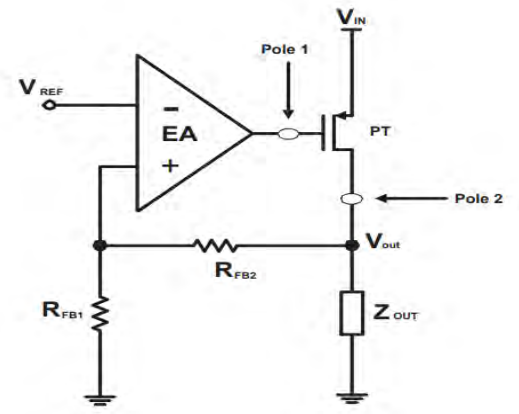

Figure 2.3: *LDO Voltage Regulator Scheme*

LDOs are compensated internally using Miller and other approaches. Compensation based on a single active loop requires at least three gain stages to boost LDO open loop gain, while multiple loop designs enhance slew rate at the gate of pass transistor. The primary benefits and drawbacks of internal compensation are:

Advantages

- It increases transient response and maintains AC stability.
- It is possible to integrate it entirely into a system on a chip, also known as a SoC.

Disadvantages

- The additional block, which might be either the current amplifier or the slew rate enhancement circuit, leads to a rise in current consumption.

- Increased chip size. The selection of a topology and appropriate compensation associated with an LDO voltage regulator is contingent upon the preferences of the designer. Subsequently, an examination of several internal compensation strategies is undertaken.

2.5 State-Of-the-Art Research

The output-capacitor less LDO (OCL-LDO) has garnered lot of interest in the realm of System-on-Chip (SoC) applications, amidst many LDO architectures. In contrast to conventional low-dropout regulators (LDOs), the on-chip linear regulator with output capacitor-less (OCL) design eliminates the need for a large external capacitor with a capacitance on the order of microfarads ($\approx \mu$F). In turn, there are benefits in both the chip and PCB space, as well as the cost of components.

Nevertheless, the task of ensuring stability control for OCL-LDOs becomes increasingly complex once the hefty output capacitor is eliminated. In contrast to conventional low-dropout (LDO) regulators, the dominant pole of the output capacitor-less LDO (OCL-LDO) is produced mainly at the power transistor's gate, whilst the non-dominant pole is linked to the output node [13]. In addition, the proximity between the dominant pole and non-dominant pole in OCL-LDOs has presented significant stability issues with their design, particularly under mild or zero loading circumstances. In order to address this particular challenge, various on-chip compensation solutions have been suggested for OCL-LDOs, which involve the utilization of small compensation capacitors with a capacitance in the range of about picofarads. Still, a significant number of these systems continue to experience poor stability when subjected to small or no loads. Additionally, their regulation performance is constrained due to the utilization of a simplistic two-stage loop design.

In an on-chip linear dropout regulator (OCL-LDO), the value of the output capacitor C_L is mostly determined by the parasitic elements present in the power line. Consequently, the value of C_L is significantly smaller compared to the off-chip capacitor typically used in a conventional LDO, which is commonly represented by a range of 10 to 100 pF. The loop response of an

OCL-LDO is crucial to its performance [2]. Enhanced transient response and power supply rejection (PSR) can be achieved with an increase in loop gain magnitude and a broader unity-gain bandwidth (UGB).

On the other hand, the benefits of technology scaling are leading to higher bandwidths in RF and communication circuits. To date, the requirement of quiescent current (IQ) for obtaining high current efficiency has limited the frequency of OCL LDOs to low levels (usually below 10 MHz). Two OCL-LDOs with loop bandwidths greater than 100 MHz are mentioned in these sources. The tri-loop LDO in [reference] has a -20 dB PSR at low frequencies, and only one of its three loops achieves above 100 MHz UGB with a DC gain of merely 20 dB. This is tenfold lower than other systems. Its transient response is constrained by a loop bandwidth of less than 20 MHz. Despite being designed using 65-nm technology, it can only produce a maximum of 10 mA of output current.

In recent years, a number of strategies have been put forth with the aim of enhancing transient responses through the use of control circuits that exhibit rapid response times while also maintaining low power consumption [14]. [15], suggests an LDO architecture that achieves quick transient response by utilizing a flip-flop voltage follower (FVF) and eliminating the need for a high-bandwidth output capacitor. Although the utilization of a low loop-gain architecture leads to reduced regulation accuracy and inadequate power supply rejection (PSR) while operating at lower frequencies, The LDO architecture described in[16] , demonstrated a rapid transient response by utilizing a comparatively high quiescent current (IQ) of 6 mA, which was effectively regulated by an on-chip capacitor with a capacitance of 0.6 nF. But this particular strategy results in a decline in the existing efficiency (η_C) during periods of low load while also requiring a substantial amount of chip space. This is not ideal for low-powered applications or system-on-chip (SoC) applications with restricted size.

The paper[16] introduces a novel Low Dropout Regulator (LDO) design with improved transient performance, achieved through Single Miller Capacitor Feed forward Compensation (SMFFC). This innovation enhances the gate slew-rate of the power transistor, resulting in better transient response during

rapid load current changes. The LDO, fabricated using 130nm CMOS technology, occupies a remarkably compact area of only 0.0113mm². Experimental results demonstrate its stability for load capacitances as low as 0pF across a full load range of 0-50mA. Additionally, when the load current shifts from 1mA to 50mA, the LDO can restore its output voltage within 190ns with a minimal voltage spike of less than 75mV. This design is particularly well-suited for VLSI implementations, offering improved performance, reduced silicon area usage, and addressing issues related to bandwidth and slew-rate limitations commonly found in conventional LDOs.

The paper [17] introduces an output-capacitorless Low Dropout Regulator (LDO) with enhanced transient response. This is achieved by incorporating a push-pull buffer that can deliver substantial charge and discharge currents to the power transistor gate, thereby improving the slew rate. An adaptive resistance unit is also integrated to address stability issues associated with Miller compensation. The proposed LDO is fabricated using 0.18-micrometer CMOS technology and demonstrates a low quiescent current of 16.1 microamperes. It regulates 1.5V output from a 1.8V supply, with a maximum dropout voltage of 300mV at 50mA load. The voltage spike is limited to 129mV, and the recovery time is swift at 0.2 microseconds. This innovative LDO design combines low power consumption and rapid transient response, making it highly suitable for stabilizing power supply in compact electronic devices

An innovative low-dropout regulator (LDO) that is specifically designed for use with system-on-chips is presented in [17] The aforementioned LDO makes use of an innovative Q-reduction circuit, which allows for a major decrease in both the on-chip capacitance as well as the optimum output current. Despite its implementation in a typical 0.35 μm CMOS technology, the LDO has achieved this decrease in productivity. This inventive design brings the on-chip capacitance down from 25 pF to 6 pF, and the results of the experiments show that it can regulate voltage down to 1.2 V with a dropout voltage of 200 mV while producing a maximum output current of 100 mA. Because of the one-of-a-kind architecture of the LDO and the integrated Q-reduction circuit, the chip area can be made more compact, and the minimum output current requirement can be lowered. As a result, the LDO is an excellent choice

for progressing SoC designs that call for effective local voltage regulation.

To enhance load and line regulation as well as the stability margin, a second feedback loop in [18] regulates the bulk voltage of the output transistor. Adding an extra amplifier with reasonable voltage gain and a wide bandwidth is employed to drive the bulk of the pass device, which is illustrated in Fig. 1(b), which alters the basic architecture. However, this amplifier raises the regulator's quiescent current. In order to lessen the size of the gate and boost regulation capabilities, the forward body bias (FBB) is used for the output device in [19]. Extra power will be required because of the necessity of an extra circuit that was not included in this paper. In addition, the error amplifier's heavy reliance on cascading which has a substantial adverse effect on the minimum input voltage, which is in fact capped at 2.8 V.

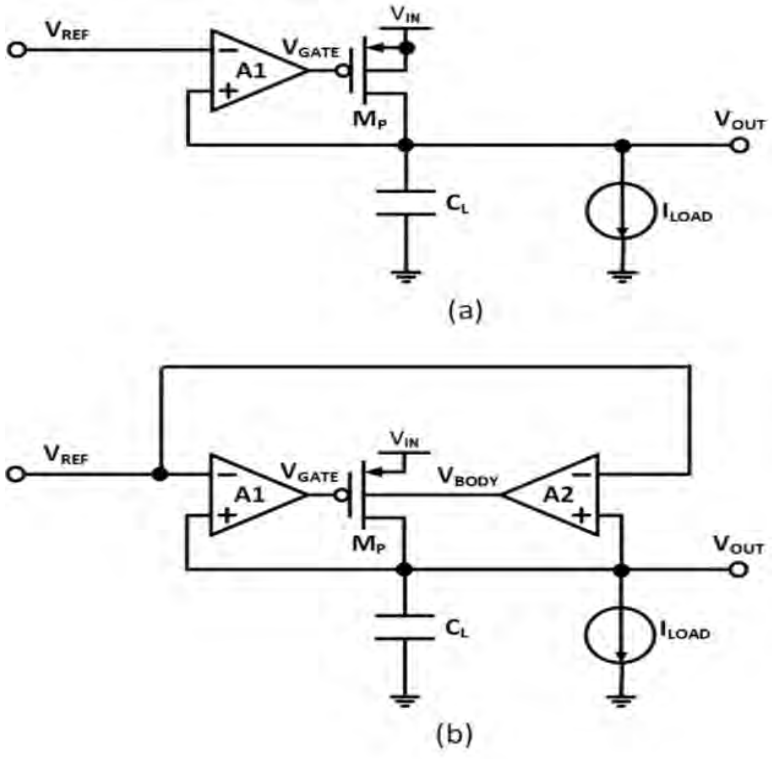

Figure 2.4: *Schematic of LDO with unity gain feedback: : (a) without body bias control and (b) with bulk-modulation.*

In[20], the study offers a straightforward and space-efficient low-dropout (LDO) architecture that utilizes a flipped-voltage follower (FVF). But the low

loop gain associated with this approach leads to inadequate regulating accuracy. On the other hand, it is worth noting that stability can still be obtained without the need for an additional compensating capacitor. The improved flipped voltage follower (FVF) described in [21] utilized a configuration consisting of four stacked cascoded transistors to attain accurate regulation along with a high gain. However, this design demands a greater voltage headroom, leaving it unsuitable for contemporary low-voltage applications. Hence, the task of designing a low-dropout regulator (LDO) that satisfies all the required performance parameters poses substantial barriers.

In [22], adaptive biasing adjusts the bias current of the op-amp based on the load current.The most effective application of adaptive biasing is when it is used to make the LDO stable across the whole current range. This is accomplished by decreasing the bias current of the operational amplifier when it is driving a light load and raising it while driving a heavy load. As a result of this, the power consumption is decreased because the op-amp now only draws a large current when it is connected to a heavy load.

Figure 1 depicts a general categorization of low-power design strategies for enhancing transient response into four components. The first problem is the use of non-static biasing techniques to maintain maximum current efficiency at low load. Adaptive biasing is used, for instance, in whereby load information is used to dynamically change the bias current.

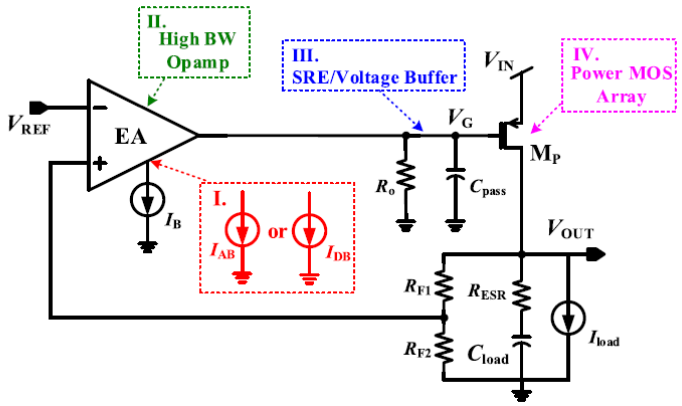

Figure 2.5: *Typical circuit techniques for fast-transient LDO design*

In any case, the adaptive function is only activated as the gate voltage V_G is reduced. When there is a transition in load from a light load to a high load, the limited bandwidth at light load might result in a visible time delay before the voltage V_G decreases and the adaptive biasing mechanism is triggered. This delay greatly reduces the efficacy of the attraction. An alternative approach, known as dynamic biasing [23]–[24], has been developed to improve response time by employing capacitive coupling while minimizing power consumption. Consequently, the stability of this loop ends up significantly more complicated due to the addition of an extra nonlinear loop during the transient phases. Second, in order to enhance the loop bandwidth of the low-dropout (LDO) regulator, the employment of EA architectures with characteristics such as high bandwidth, low quiescent current, and area-efficient internal compensation techniques has been followed. These strategies encompass damping factor control [25], Q-reduction compensation [26], and other advanced frequency compensation techniques that enable adjustment of internal pole-zero positions [3]–[6]. Since amplifiers with multiple stages have proven effective,the complex mathematical analysis of the frequency response has provided a challenge for the rapid design of circuits. The implementation of a single-stage amplifier design, which includes an operational transconductance amplifier (OTA), is more likely to be favored due to its beneficial single-pole characteristic [27], [8]. But still, the drawback of this approach is the trade-off in terms of quiescent current, which is affected by the presence of several cascaded (CA) stages. Third, the V_G gate-source (SR) can be enhanced by implementing a slew-rate-enhancement circuit or voltage buffer, which in turn shifts the associated parasitic pole to a higher frequency. Fourth, the Pass transistor (Mp) can be effectively divided into a power MOSFET array, which serves the purpose of facilitating loop compensation while ensuring smooth pole tracking. Transient enhancements can be achieved by the use of dynamic biasing, as seen in [3]. The bias current of the op-amp only fluctuates rapidly at transients in the output voltage and then returns to its steady state value. To mitigate voltage overshoot and undershoot in capacitor-less LDOs, various transient boosting circuits have been developed. PMOS LDOs use direct voltage-spike detection, EAs along with input cross-coupled CG transistors and output current

summing stages, multi-loop control was developed in , and slew rate enhancement techniques are applied in [27]. The literature review shows the fact that the quick transient approach is crucial for offering a stable supply voltage even at high loads, with minimal overshoot and undershoot of the output voltage, high efficiency, and low silicon footprint.

Chapter 3

Capacitor-Less Low Voltage Regulator Design with optimized undershoot and overshoot

A comprehensive approach for designing a CMOS analog circuit-supplying fully integrated LDO is studied in this chapter. The low-dropout (LDO) regulator implemented in this study is designed using the 55nm bulk CMOS technology within the Cadence Virtuoso platform.

Following a description of the fundamental LDO topology, a small-signal model is formulated, describing the pass-transistor and error amplifier's full open- and closed-loop transfer functions. On the basis of this regulator model, an overview of the LDO specifications is given, including factors for DC performance and small-signal AC performance.. Concerning this, the primary constraints and tradeoffs of LDO design are highlighted.

3.1 Studied LDO Architecture

The objective of this phase of the initiative is to develop a capacitor-less low-dropout (LDO) regulator specifically designed for system-on-a-chip (SoC) applications.Ensuring circuit stability across all loading currents, particularly during low-load currents, is of paramount importance. Additionally, it has to be

required that the circuit exhibit optimal responses to rapid load changes. The purpose of the design guidelines is to reduce power and area consumption while ensuring satisfactory regulation performance using a low-voltage topology. These guidelines are tailored to meet our specific requirements, which include achieving a 1.2 V output voltage (Vout) that is compatible with battery supply voltage values (VBAT) ranging from 3.3 V to 1.3 V across a temperature range of -40 to 120 degree Celsius. Additionally, the design should support a maximum load current (ILoad) of 50 mA and accommodate a maximum load capacitance (CLoad,max) of 10 pF. In the present work, we have implemented the compensation and dynamic-enhancement techniques that were previously successful in a [], but we have made changes to ensure compatibility with low-voltage requirements. Besides that, we have further improved the transient response by including a multiple-dynamic feedback strategy.

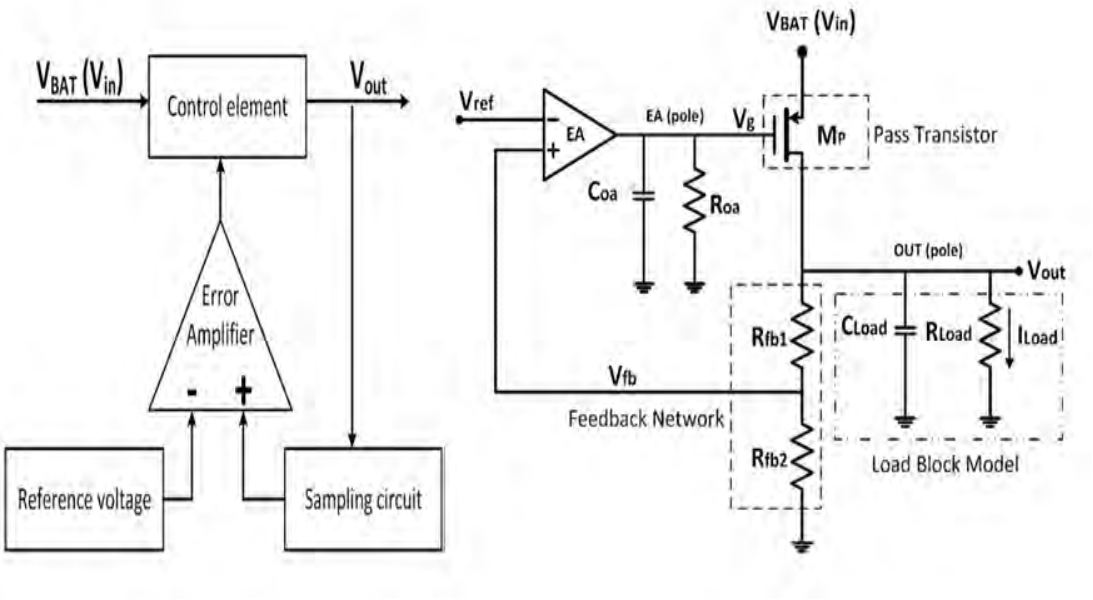

Figure 3.1: *(a) Linear regulator conceptual scheme (b) A simplified schematic of a CMOS low-dropout (LDO) regulator.*

Figure 3.1(a) depicts a simplified arrangement of a CMOS linear regulator, which converts an unregulated input voltage Vin (the battery voltage VBAT) into a regulated output voltage Vout for the PMU of a battery-powered portable

device [29].The suggested LDO has a 1 pF internal capacitor, an error amplifier, a PMOS pass transistor, and a system of feedback with two feedback resistors. In accordance with Fig. 3.1(b), A sampling network is used to take a small sample of the output. To drive the gate of the pass transistor, an error amplifier compares Vfb and Vref and amplifies the difference (which is supposed to be an error). As a result, VGSpass is not a constant but rather varies with the output voltage. As Vout rises, so does Vfb, resulting in a larger inaccuracy (relative to Vref). This error gets amplified to the pass transistor's gate, lowering VGSpass in direct proportion. In order to compensate for the excess in the output voltage, the operating point can be moved by lowering VGSpass to a value where the voltage drop across the pass transistor rises while the load current remains constant. The output load current is presumed to be an ideal current source.

For an ideal op amp, gain is infinite and differential input is zero.

$$V_{fb} - V_{ref} \approx 0 \tag{3.1}$$

$$(R_{bf2}/R_{bf1})V_{out} - V_{ref} \approx 0 \tag{3.2}$$

$$V_{out} = (1 + R_{bf2}/R_{bf1})V_{ref} \tag{3.3}$$

In the suggested circuit, the topology of the first stage correlates to a two-pole system, with one pole situated at the pass transistor's gate:

$$f_{out} \approx \frac{1}{2\pi R_{oa}(C_{oa}||R_{oa})} \approx \frac{1}{2\pi R_{oa}C_{gsp}} \tag{3.4}$$

Both Roa and Coa define the error amplifier's output impedance and C_{gsp} is the PMOS pass transistor's gate-source capacitance. The other pole is situated near the output of the low-dropout (LDO) regulator and is determined by:

$$f_{out} \approx \frac{1}{2\pi R_{oa}(C_{oa}||R_{oa})} \approx \frac{1}{2\pi R_{oa}C_{gsp}} \tag{3.5}$$

For a steady SoC LDO regulator, locate the dominant pole at the error amplifier output f_{EA} . Provided that the pole situated at the output must meet the condition of $f_{out} >> f_{EA}$.

3.2 The fundamental structure:

In this section, we will detail the circuit's core (Fig.3. 2) and the implementation of the enhancement structure (Fig. 3.5), to realize the capacitor-less LDO regulator. This sort of regulator functions similarly to a voltage source, keeping the output voltage stable regardless of load or battery voltage fluctuations.

The schematic diagram depicted in Figure 3.2 , which encompasses a PMOS pass transistor (MP), a resistive feedback network, an EA, and a reference voltage (Vref) set at 0.4 V. For the purpose of ensuring the PMOS transistor operates in saturation mode, with the highest possible load current (ILoad) of 50 mA and a dropout of 200 mV, its dimensions are configured to be 4 mm in width and 2000 nm in length. To mitigate the parasitic capacitance of the gate pass transistor, denoted as CgsP, efforts are made to decrease its value. Under no load conditions, CgsP is approximately 15 pF, while it can increase up to 18 pF under maximum load. This is achieved by employing the smallest permissible transistor length as dictated by the 55nm technology.

In an effort to maintain low power consumption, the pass transistor's static current is configured to operate at 1.5 μA during periods of no load. This strategy is applied to achieve energy efficiency while ensuring the output voltage (Vout) remains at 1.2 V, aligning with a reference voltage (Vref) of 0.4 V. The arrangement of resistive components involves a pair of resistors, namely Rfb1 and Rfb2, with their combined resistance amounting to 800 kΩ. Notably, Rfb1 holds a value twice that of Rfb2. To optimize spatial efficiency, this resistance network is constructed using three identical low-voltage PMOS transistors in diode configuration within a Psubstrate N-well technology ,referred as $(M0, size3\mu m/10\mu m, withVBS = 0)$. This specific implementation results in a significant reduction in occupied area, approximately 250 times smaller compared to using a highly resistive polysilicon layer (characterized by $(Rsquare = 1039\Omega/square)$. within the technology framework.

Telescopic op-amp, folded cascode op-amp, two-stage op-amp, etc. are just a few examples of the many different topologies that op-amps can take [5]-[7]. In this study, we present the design of a folded cascode op-amps circuit that is entirely differential. NMOS and PMOS transistors are two examples of

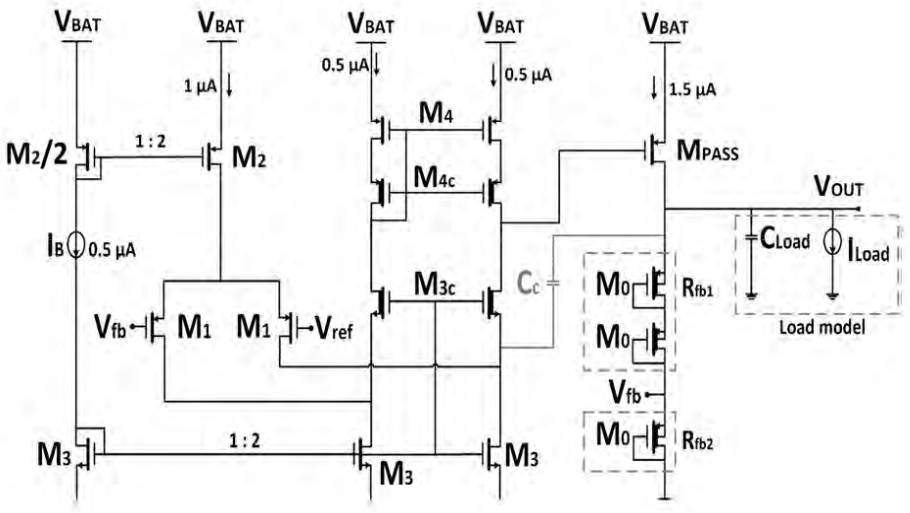

Figure 3.2: *The fundamental architecture of the CMOS low-dropout (LDO) regulator designed for generating a 1.2V output.*

signal channels that can be folded to create a cascode [1].A folded-Cascode PMOS-Input differential pair is realized in this work.One of the most useful characteristics of folded cascode op-amps is their ability to accept input common-mode levels that are extremely close to the supply voltage. The input common-mode voltage can be reduced to 0V with a PMOS input. Folded cascode is a single-pole op-amp with more gain and wider output swing than conventional op-amps. The higher phase margin as well as the stability offered by single-pole op-amps are two of their primary benefits [16].All of the DC gain required to fulfil the power supply rejection and the line regulation specification is provided by the design's single-stage folded-cascode error amplifier (M1–M4). Additionally, the output voltage swing meets the dynamic requirements under heavy load.

The utilization of low-voltage transistors, which are inherent to the technology, is employed for the cascode transistors. A self-biased scheme is implemented, wherein the gates of M4 and M4C are interconnected, as well as the gates of M3 and M3C. This approach eliminates the need for supplementary bias branches, as depicted in Figure 3.2. The remaining transistors within the circuit operate at a standard voltage of 3 V. Figure 3.3 illustrates the schematic

representation of each of the two transistors, namely the native transistor and the regular transistor, together with their primary properties.

Transistor	Regular	Native
Schematic		
Vds,max	3.3 V	3.3 V
NMOS (V_{th})	0.592	0.068
PMOS (V_{th})	-0.72	-0.42

Figure 3.3: *Characteristics of Transistors*

The Error amplifier acts with a total current of 3.5 μA, which includes a bias current of 0.5 μA. It demonstrates a gain greater than 70 dB, a phase margin of 89 degrees, and a gain-bandwidth product exceeding 104.4 MHz. These characteristics remain consistent across the battery voltage range of 1.3 V to 3.3 V. As soon as the load current is low, the output frequency f_{OUT} tends to be near f_{EA}, resulting in a decrease in the phase margin to 32^o. This value is below the Barkhausens' limit of $(45^o - 60^o)$, as indicated in reference [32]. The cascode Miller compensating technique is employed in this device to enhance its resilience. The compensation capacitor is responsible for dividing the poles at the output of the error amplifier and the output of the low-dropout (LDO) regulator, denoted as V_{out}.

3.3 Design Challenges

To make an LDO that uses little power and has no capacitors on the outside, there are some obstacles. First, low power consumption lowers LDO dc and ac performance. This study limits the biasing current of the error amplifier inside the LDO to roughly 5 μA to reduce power consumption. This limited biasing current causes the error amplifier's output impedance to be high, resulting in a low-frequency pole that impairs the LDO's bandwidth, stability, and transient response. Due to the inverse relationship between current and resistance, the

large output impedance of the error amplifier is another consequence of the low biasing current. The pass transistor's huge parasitic gate capacitance and large output resistance combine to form a dominating pole at a very low frequency. The stability of an LDO degrades when its dominating pole moves to lower frequencies. The formula for r_{ds} is:

$$r_{ds} = \frac{1}{\lambda I_D} \tag{3.6}$$

In addition, the restricted power limitations impose constraints on the accuracy of the low-dropout regulator (LDO) at the output due to the fact that the gain of the error amplifier is directly proportional to the bias current. The LDO's direct current (dc) performance, including load and line regulations, is negatively affected by the low open loop gain resulting from low power consumption. A further major hurdle is that the traditional low-dropout (LDO) regulator requires a large off-chip output capacitor that possesses an equivalent series resistance (ESR). The inclusion of an equivalent series resistor in the circuit of a low-dropout (LDO) regulator serves to counteract the presence of a second pole, effectively canceling it. This cancellation of the second pole is advantageous as it promotes stability in the system.

In the context of transient response, the addition of a large output capacitor helps decrease the occurrence of undershoot during instances of rapid load transients. Because the big capacitor gives the current a fast way to get to the load right away until the LDO can respond to the output load glitch and change the current via the pass transistor. But the LDO that doesn't have an external capacitor only has one small capacitor on-chip and no ESR. Because the output capacitor is small, the pole at the gate of the pass transistor becomes the dominant pole, whereas the pole at the output becomes the non-dominant pole.

The stable operation of the LDO must be compensated because the output pole varies with load, and this is especially true in the no-load condition, when the non-dominant pole is at a very low frequency, reducing the phase margin of the entire system. High undershoot is seen throughout output load transients because the tiny on-chip capacitor is unable to supply a rapid current

path for any fast changes in load.

3.4 Transient Response

Analysis of transient load regulation without a circuit to boost the dynamical characteristics reveals that the corresponding LDO circuit produces substantial settling time and voltage peaks (Figure 3.4). This offers overshoot (OS) and also undershoot (US) voltage peak levels of about 0.7 V (OS) and 0.95 V , respectively. These figures highlight the importance of a transient control circuit that can stabilize the output voltage quickly with low voltage peaks while still adhering to space and power efficiency requirements.

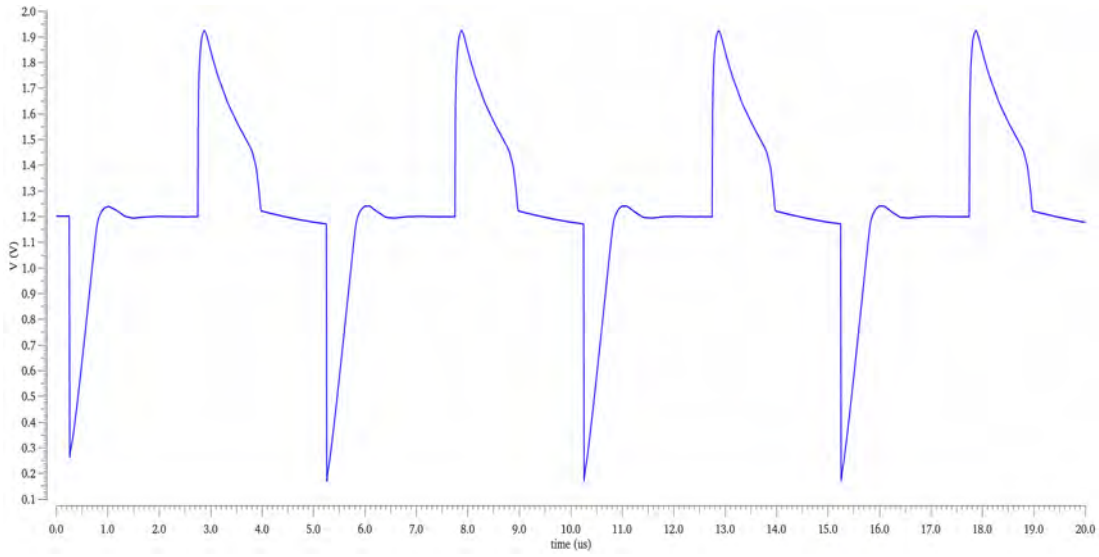

Figure 3.4: *Transient behavior of the load, between 0 to 50 mA, with VBAT = 3 V and no transient augmentation.*

The dynamic transient response of an LDO system is reliant upon the error amplifier's loop bandwidth and the slew rate. In addition to the slew rate, a reduction of undershoot (US) and overshoot (OS) in a low-dropout regulator (LDO) can be achieved through the incorporation of an additional circuit for detecting output voltage US and OS. The primary objective is to promptly detect voltage glitches at the output prior to the loop responses and instantly implement the bias changes to the power transistor's gate.

The circuit for detecting overshoot transients involves the utilization of an NMOS quasi-floating gate (QFG) transistor, denoted as MQFG, N. The gate voltage of MQFG,N is established by a DC bias VBN and is coupled to a high resistance, which is implemented by two PMOS transistors arranged in a diode configuration being reverse biased. A capacitor, CQFG = 1 pF, connects the output node to the QFG transistor. In a steady state, the voltage between the gate and source denoted as VGS and VBN, is measured to be 0.4 V, which is less than the threshold voltage VTH, N, of 0.59 V. Consequently, the metal-oxide-semiconductor field-effect transistor MQFG,N remains in the cut-off zone, exhibiting minimal leakage current usage. Depicting the equation as VGS = VBN = 400mV $<$ VTH,N = 0.59 V, In the case of a quick drop in ILoad, the resulting overshoot at Vout becomes coupled through CQFG, so initiating a triggering effect on the transistor and subsequently producing a current. This current goes straight to the lower Ibias branch of the error amplifiers at node C, which helps the gate capacitance CPASS in charging. Furthermore, MQFG, N is replicated to MQFG, N' so that it can proactively sink more current at the LDO's output. This helps discharge the path that is established by (Rfb1 + Rfb2) plus CLoad. MQFG,N will return the cut-off mode once it has been adjusted so that Vout will once again be at its nominal value.

Another circuitry made up of two matched QFG PMOS transistors MQFG,P is employed to serve undershoot (US) transient detection. once more a 1 pF CQFG capacitor is placed between Vout and a DC bias voltage VBP via the voltage gate. As long as the gate voltage is maintained at VSG = (VBAT - VBP) = 0.55 V —VTH,P— = 0.72 V, the transistor will continue within the cut-off mode. Subsequently, when the output voltage (Vout) experiences a sudden decrease, the resulting change is transmitted to the gate of the MQFG,P transistors. This causes the gate-to-source voltage (VSG) to exceed the absolute value of the threshold voltage (—VTH, P—), thereby enabling the transistors to switch into the "active" region of operation. The CPASS discharge of the gate capacitance is sped up by the right-away generated currents, which are added to the upper Ibias branches at points A and B of the error amplifiers. MQFG,P will revert to its off state after the bare minimum amount of Vout has been restored.

In order to enhance the transient behaviour of (US), an alternative approach known as the Transient Enhancement Circuit (TEC) is depicted in Figure 3.5. This approach involves the incorporation of dynamic current sources, denoted as MDB, which are connected in parallel to the currents at nodes A and B. The TEC is represented by the red line in the figure. In a steady state, the gate voltage of the main differential pair (VG, MDB) is equal to the gate voltage of transistor M2 (VG, M2), while the transistors are operating in the saturation region and generating a constant current of 1 μ A each. When the output voltage (Vout) lowers, the fluctuations in voltage are connected to the gate of the device through a capacitor (CQFG), which speeds up the discharge process.

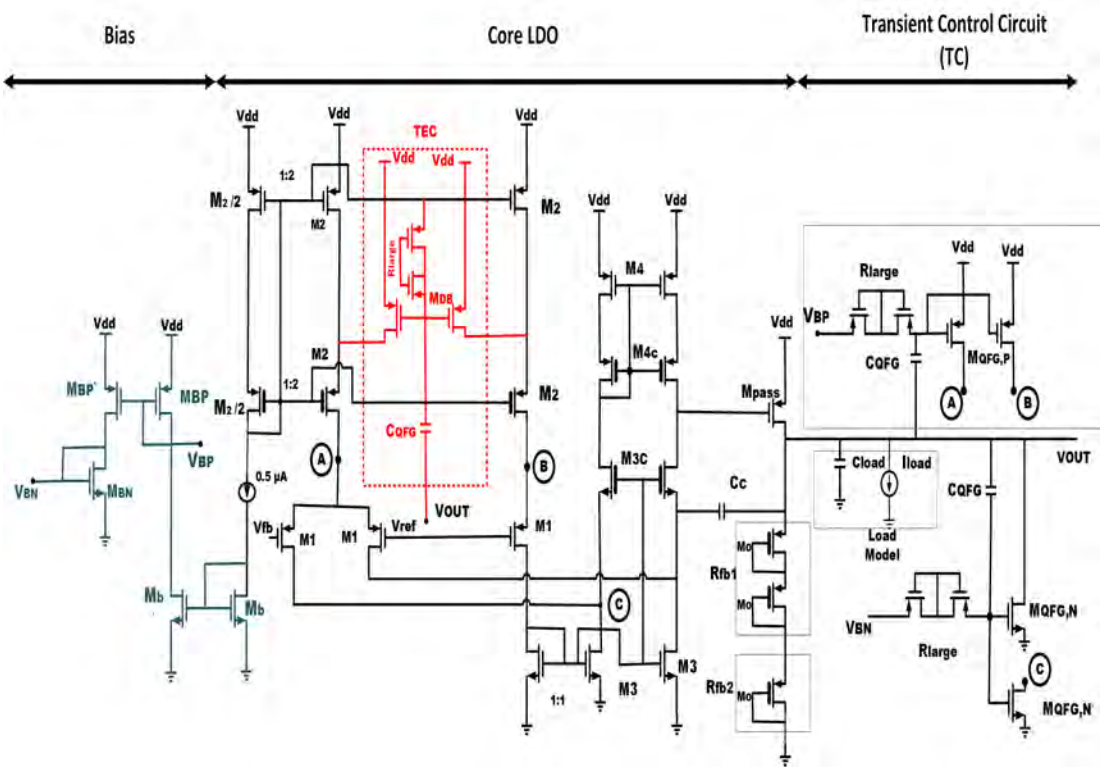

Figure 3.5: *Low dropout regulator core construction with transient control circuitry*

3.5 Simulation Environment

The low-dropout (LDO) regulator in this study has been implemented utilizing the 55nm bulk CMOS technology within the Cadence Virtuoso platform. Table 3.1 provides a comprehensive summary of the design parameters, including the (W/L) values of all MOSFETs and the capacitor values depicted in Figure 3.

The calculation of the overall aspect ratio of the suggested design is determined by employing Equation 1.7, which refers to the saturation region of MOSFETs.

Table 3.1: Aspect Ratios of the Transistors

Parameter	**W(μm)**	**L(μm)**
M_1	60	0.34
M_2	15	3
M_3, M_{3c}	16	2
M_4, M_{4c}	9	3
M_{pass}	4m	0.2
M_0	3	10
M_{DB}	1.5	0.5
R_{large}	50	5
$M_{QFG,BP}$	3.70	0.07
$M_{QFG,BP'}$	3.70	0.07
M_{BP}	25	0.06
$M_{BP'}$	25	0.06
M_{BN}	10	0.06
Mb	4	1
$M_{QFG,P}$	3.704	0.07
$M_{QFG,N}$	3.704	0.07
$M_{QFG,N'}$	20	0.34

3.6 Design Specification

Table 3.2 summarizes the studied design's overall specifications. Maximum load current is 50mA at 3V supply voltage. At the design's output, a capacitor

with a value of just 1pf is utilized. The suggested LDO has a dropout voltage of less than 200mV.The square law approximation is employed for all calculations, unless explicitly specified otherwise.

Table 3.2: Design Specification of the LDO Regulator

Parameter	**Specification**
Input/Output Voltage	3V/1.2
Voltage Overhead	$<$ 5mV
Line Regulation	0.053(mv/V)
Load Regulation	0.0001(mV/mA)
Load Current	50mA(max)
C_{out}	1pF (on-chip)
V_{out}	1.2V

3.7 Simulation and Result Analysis

Within this particular section, we shall proceed to provide an analysis of the transient, DC, and AC parameters of the design that has been put forth.

3.7.1 DC Analysis

The DC analysis is a quantitative metric used to assess various aspects of a low-dropout regulator (LDO), including its operating region and line regulation. With the implementation of the Transient Enhancement Circuit (TEC), the undershoot and overshoot are reduced to 0.17V and 0.15V , respectively, with a settling time of 0.15μs. (see fig 3.6).

Line and load transient simulations are used to characterize the implemented LDOs' transient performance. At the input node VDD, we apply a line transient step from 1.8V to 2V with a rise and fall time of 10 ns. The test

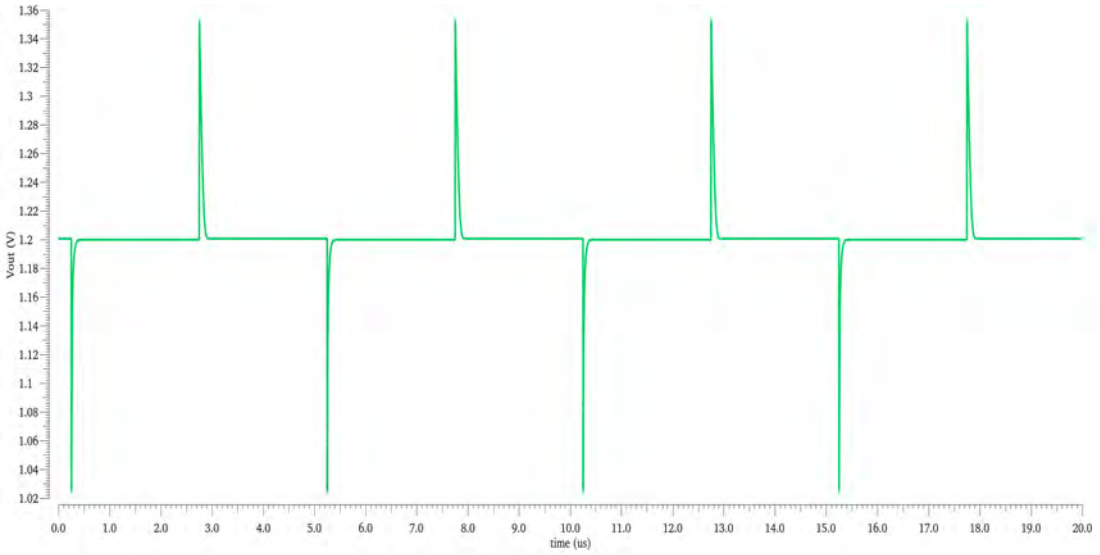

Figure 3.6: *: Measured Output Voltage of the LDO Regulator with C=0 pF*

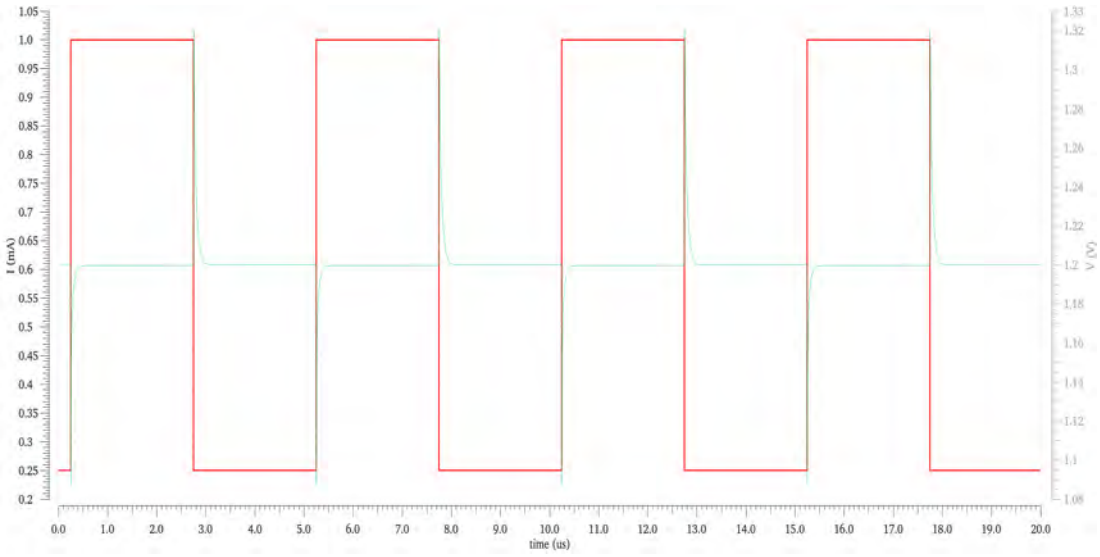

Figure 3.7: *LDO transient response and Iout on the load step from 50mA to 10mA*

was conducted with a continuous load current (IL) of 1 mA. As can be seen in Fig. 3.7, the output node VOUT displays a reaction to the line transient.

3.8 AC and Stability Analysis

Figure 3.8 displays the frequency response of the circuit. The error amplifier in the two-stage configuration has a gain of 73.33 dB and a phase margin of 82.83 degree ensuring a good GBW product of 104.40 MHz.

The overall gain of the entire system is approximately half, as the output voltage (Vout) is provided to the error amplifier via resistive feedback network. This suggests that the system as a whole remains stable when subjected to full load conditions. A lowest loop phase margin of 68 degrees is attained under all bias situations.

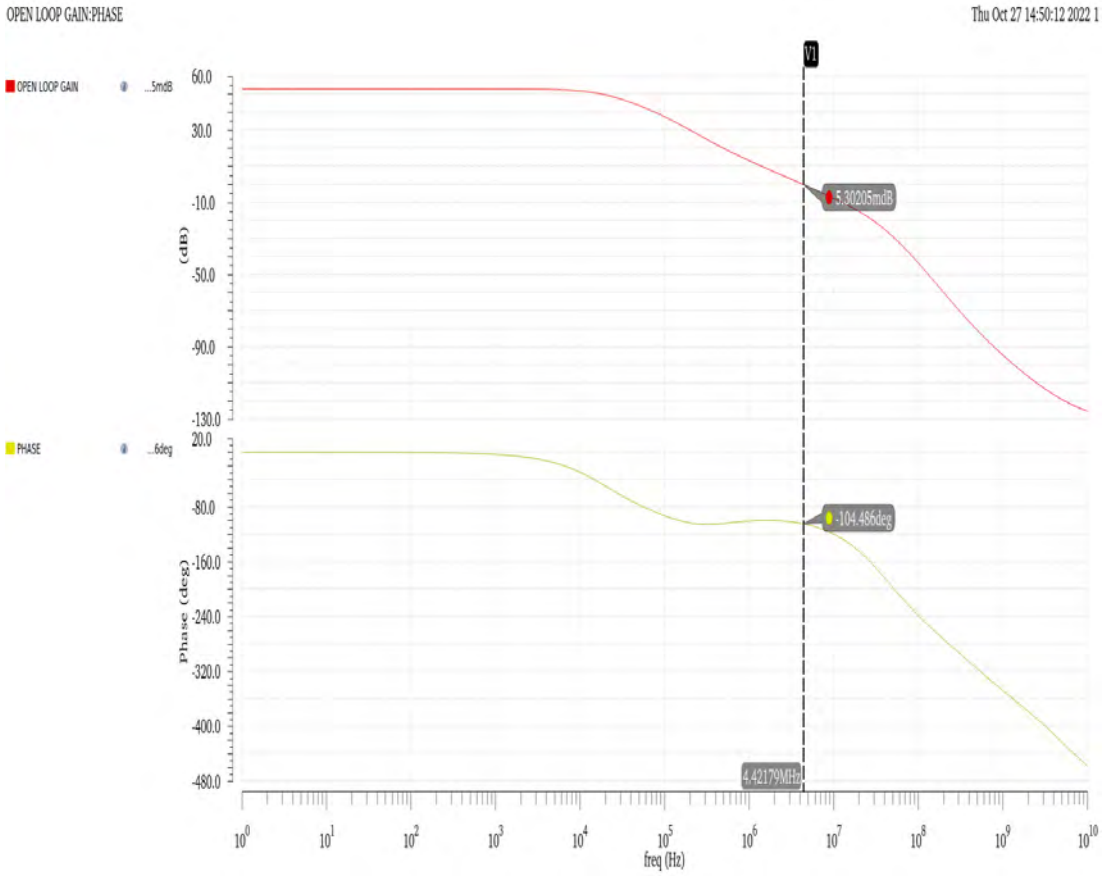

Figure 3.8: *Frequency response of the single stage error amplifier*

3.9 Line Regulation

Line regulation refers to the proportional variation in the output voltage in response to a specific change in the battery voltage. In order to assess the line regulation of LDOs, a DC analysis is conducted to examine the fluctuation in output voltage resulting from variations in the input supply voltage.

Figure 3.9 illustrates the corresponding outcome. The line regulation is determined to be 0.053 (mV/V). This implies that any alteration in voltage at the input results in a corresponding alterations of the output by a magnitude of merely 53 millivolts.

Line regulation is directly related to the loop gain, making the folded cascode architecture a good choice, as it maintains good Phase Margin.

In Fig. 3.9, you observe how the output voltage changes in a normal case when the line voltage changes.

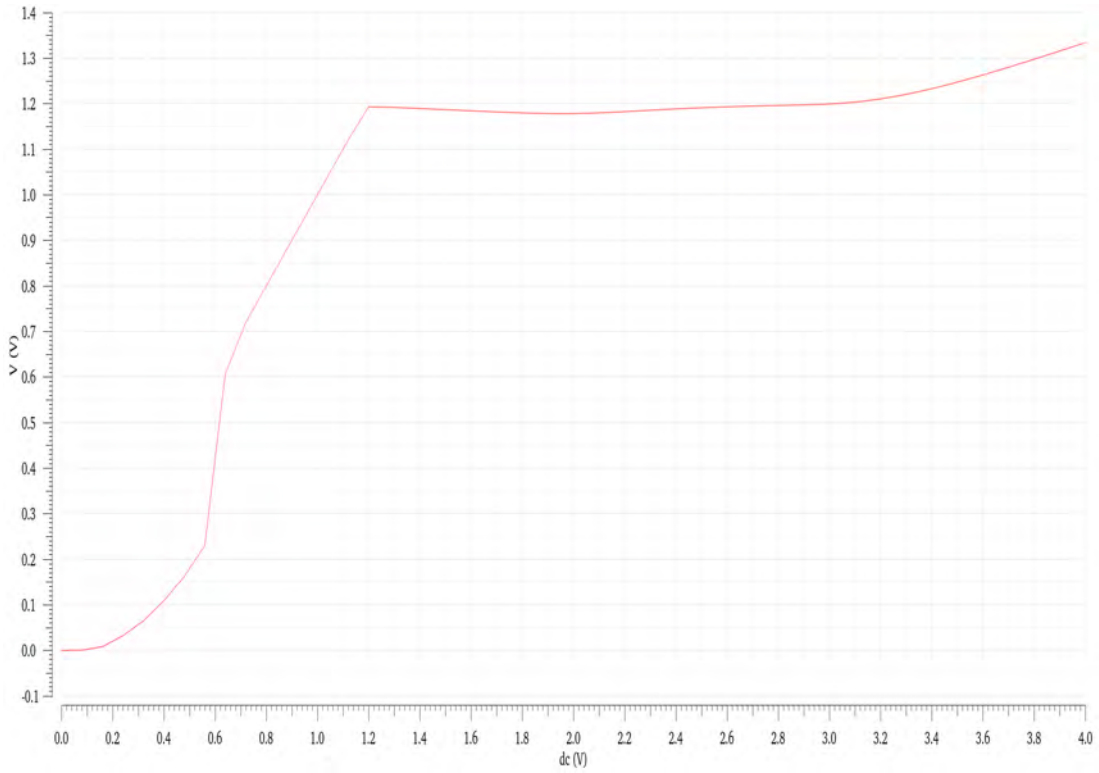

Figure 3.9: *Simulated line-transient response with a 0pF off-chip capacitor*

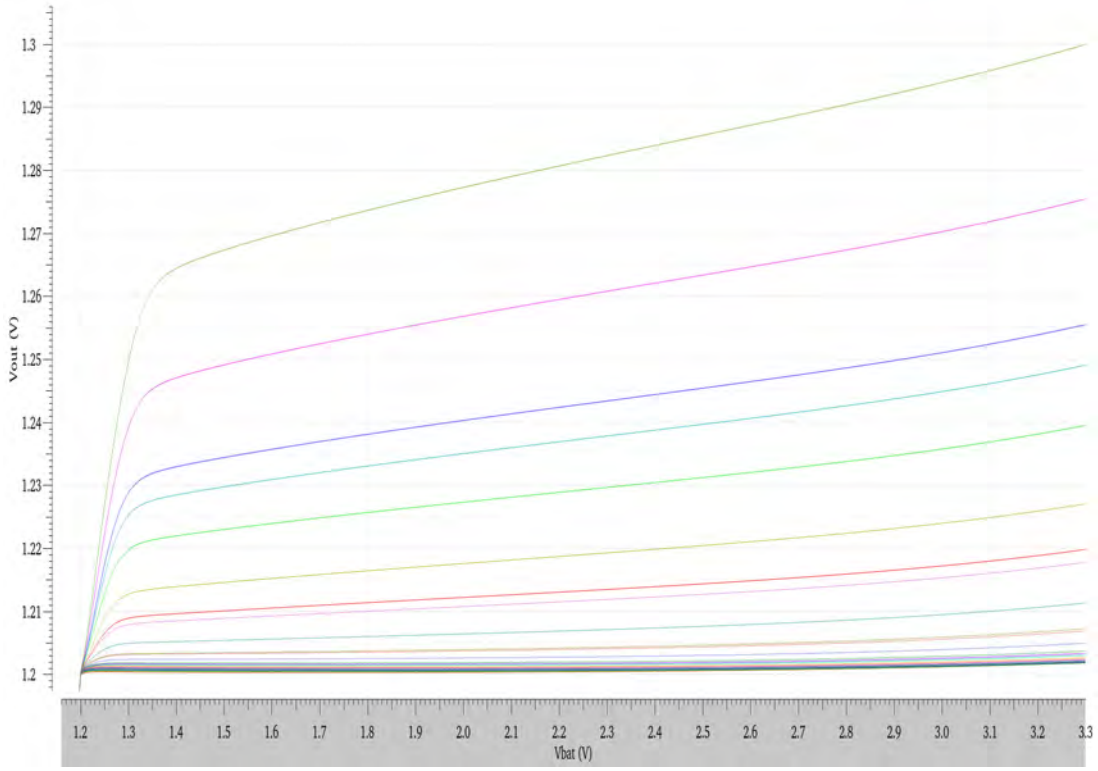

Figure 3.10: *Line transient simulation results for Temperature change from -40° to 120°and IL=1mA with CL=0 pF*

The performance of the design is analyzed at different temperatures , as depicted in Figure 3.10. The battery voltage is swept from 1.2V to 3.3V. With a temperature range of -40^oC to 120^oC , 0.1V which represents the greatest value observed. It shows minimal deviation from the desired voltage level at low temperatures.

3.10 Achieved results

Load transient Figure 3.11 illustrates the characteristic response of the output voltage in response to a transition in the current load over 0.2mA to 50mA, having rise and fall times of 1ns each. It takes approximately 100 ns for the regulator to restore the output voltage to 1.2 V. This data was obtained by simulation on CADENCE. The observed largest variation of the output voltage

from the nominal value is 150 mV in the typical scenario.

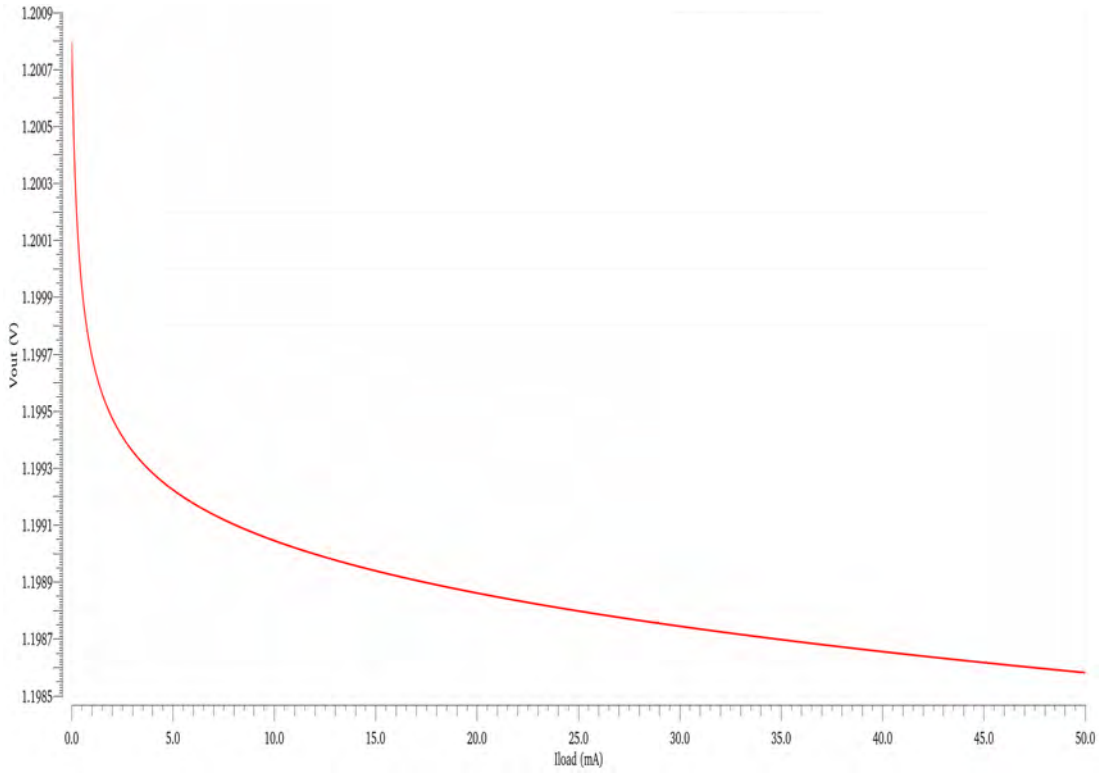

Figure 3.11: *Simulated load-transient response with a 0 pF off-chip output capacitor for different current changes ΔIload=0 to 50mA*

Current & Power consumption This LDO regulator's maximum current consumption is 59 μA at full load. The total current consumed by the LDO regulator depends on the loading current, as shown in Fig 3.7.

The LDO accepts a bare minimum of 1.3V as input and can only put out a maximum of 1.2V. This circuit consumes a total of 1 mW of power.

3.11 Layout

The complete layout of the above design is shown in Fig 3.11. The area of this LDO is 42μ x 83.7 μ.

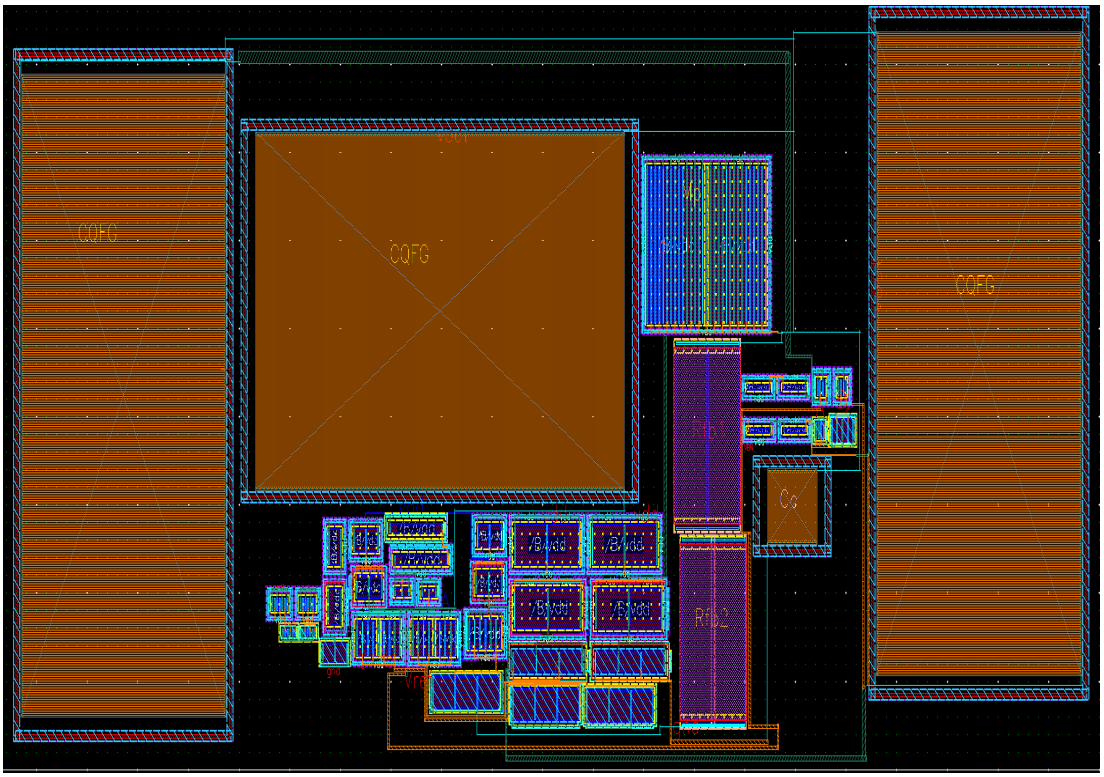

Figure 3.12: *Layout of LDO with TEC*

Chapter 4

Capacitor-Less LDO Voltage Regulator Design Using Slew-rate Enhancement

A considerable DC gain in the error amplifier is typically required for effective regulator line and load regulation. At high current loads, a single-stage error amplifier might find it difficult to provide enough gain for the DC loop. Using a multistage amplifier to increase gain makes designing a compensation circuit to maintain loop stability more difficult. Fast transient response with tiny voltage glitch at loading current fluctuations requires not only a high slew rate, but also a large loop bandwidth in LDOs. This device employs the Slew Rate Enhancement technique to strike a good compromise between speed (which necessitates a large bandwidth) and accuracy (which necessitates a large DC loop gain).

This study used an adaptive biasing error amplifier including a low-power dynamic push-pull (SRE) circuit to investigate the improvements in transient responses of a capacitor-less low-dropout regulator (LDO). It aids in mitigation of the design's reliance on restricted bandwidth and helps optimize the regulation of the power supply by reducing output voltage spikes and recovery time. The SRE circuit exclusively supplies a variable current to either charge or discharge the gate capacitance Cpass of the power transistor in the presence

of huge spikes in voltage during transients. However, it remains fully turned off in the static state, resulting in little quiescent current consumption. The enhancement of both loop-gain bandwidth and slew rate at the gate drive of a pass transistor is achieved while keeping a maximum level of current performance in a static condition.

The present chapter is structured in the following manner.The discussion of the studied LDO circuit topology and stability analysis is presented in Section I. Following the introduction of the fundamental low-dropout (LDO) topology, a small-signal model is formulated, encompassing the comprehensive open-loop transfer functions of the output capacitor-less LDO (OCL-LDO). The process of circuit design and simulation is presented in Section II. The experimental findings and conclusions are presented in Sections III and IV, respectively.

4.1 LDO Architecture

4.1.1 Implemented Topology

In Fig. 4.1, The studied OCL-LDO comprises three stages, namely an error amplifier serving as the initial stage, a non-inverting amplifier as the second stage, a Pmos transistor as the third stage, a pair of current boosters in the transient-current boosting circuitry, a frequency compensation network made up of capacitors (Cm, Ct, and gmt1), and a feedback system network. The resistance of the output load is denoted by R_L. V_C represents the source voltage to the transconductance cell gmt1. The fluctuation in the output voltage caused by load transients is coupled via the frequency compensation capacitors C_m and Ct and delivered to the current boosters, where it is amplified.

To deliver and remove additional current for charging and discharging through the transient period, the two Gm cells, which are essentially formed by two sets of matched transistors (M1 and M2 in Fig. 4.1 as an example), are cross-coupled to achieve the push-pull final stage. Since the MOS transistor's square-law characteristic dictates that its current output Io scales quadratically with the differential input-voltage of the Booster cell, the highest permissible output current I_{omax} does not need to be restricted due to the constant-current

source, unlike it would be in the case of a traditional amplifier that uses tail-current. The simultaneous achievement of low power consumption and high slew rate makes this approach highly advantageous for enhancing transient reaction in fully integrated on-chip low-dropout regulators (LDOs).

The view presented in Figure 4.1 illustrates the transient-current boosting network. During transient periods, the voltages at the positive and negative inputs of the current boosters undergo opposite changes as a result of the operation of the two separate inverters.

In other words, when there is a change in voltage, denoted as ΔV, at the positive input end of booster 1, 2, there is a corresponding change of $-\Delta V$ at its negative input end. Consequently, the overall input voltage variation, denoted as $\Delta V_{in1,2}$ is equal to double the magnitude of ΔV. This implies that the output node can achieve a high slew rate even when subjected to weak bias currents, which can be amplified throughout load transients.

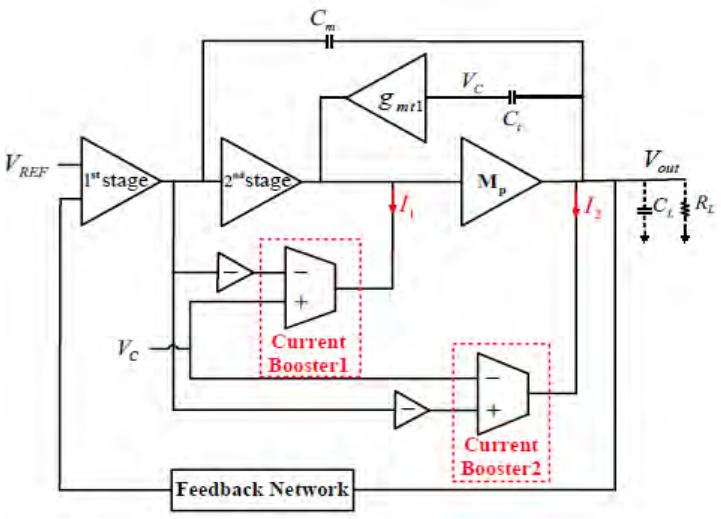

Figure 4.1: *Basic Structure of the OCL-LDO regulator*

4.1.2 Analysis of stability and design constraints

The TCFC compensation method is used to attain stability in the examined OCL-LDO. In order to provide stability alongside better recovery features at

the output node, despite changing ambient conditions, or varying process corners, frequency compensation modifies the transfer function of the LDO. The DC current demands placed on the LDO during its design span a wide range, from around 11 nA up to no more than 10 mA. Because of the huge variation in load currents, the position of the output pole changes significantly, making compensation even harder. The small-signal model associated with the OCL-LDO under investigation is depicted in Figure 4.2. According to this model, the transconductance of every stage is denoted as g_{mi}, while R_i and C_i symbolize the output resistance and combined parasitic capacitance, respectively. The non-inverting second stage is made up of g_{m2} and g_{mt}. The output resistance of the pFET M_{19} in saturation is denoted as r_{ds19}. The power mosfet's (Mp) transconductance is denoted as g_{mp}. In order to enhance the slew rate at the output node, a push-pull configuration is established by integrating a feed-forward transconductance stage denoted as g_{mf} with Mp.

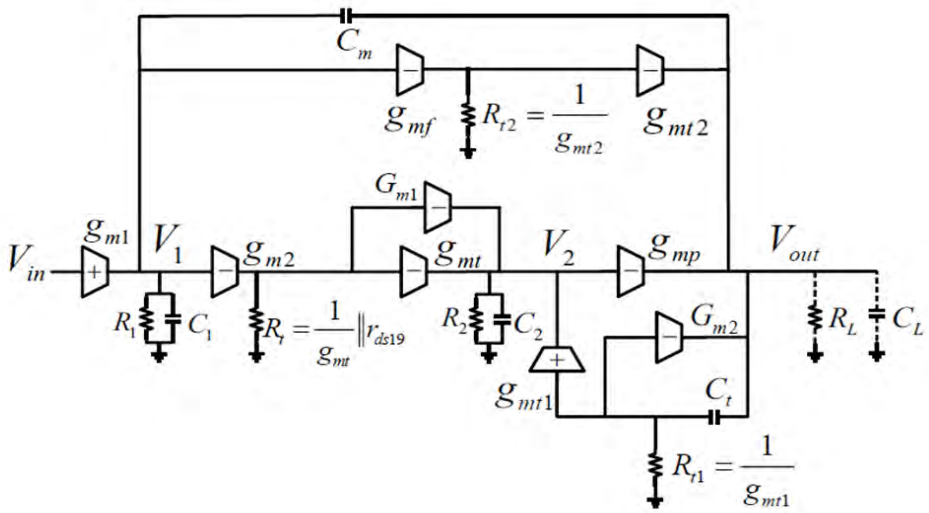

Figure 4.2: *Small Signal model of the OCL-LDO regulator*

The equivalence of the transconductance G_m of the circuit arrangement depicted in Figure 4.3 determines each G_{m1} and G_{m2}. The equation for G_m goes as follows:

$$G_m = \frac{\partial I_D}{\partial V_{in}} \tag{4.1}$$

$$G_m = \frac{g_m}{1 + g_m R_s} \tag{4.2}$$

The symbol G_m represents the transconductance of M2. In the investigated design, the parameter denoted as R_s is effectively implemented through the utilization of the r_{ds} of M15 and M21. These two nFETs operate in saturation mode, hence exhibiting substantial resistance. Consequently, the product of the transconductance (g_m) and R_s exceeds unity.

$$G_{m1} = \frac{g_{mt1}}{1 + g_{mt1}.r_{ds15}} \tag{4.3}$$

$$G_{m2} = \frac{g_{mt2}}{1 + g_{mt2}.r_{ds15}} \tag{4.4}$$

It follows that

$$G_{m1} \approx \frac{1}{r_{ds15}} \tag{4.5}$$

$$G_{m2} \approx \frac{1}{r_{ds21}} \tag{4.6}$$

The present impact of G_{m1} and G_{m2} are negligible relative to g_{mt} as well as g_{mt1}, thereby they must be omitted. Figure 4.4 depicts an updated version of the small-signal framework presented in Figure 4.2.

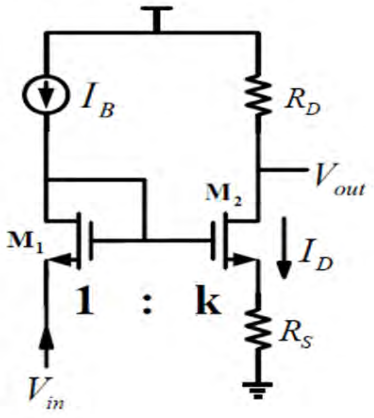

Figure 4.3: *Equivalent transconductance cell (Gm) model*

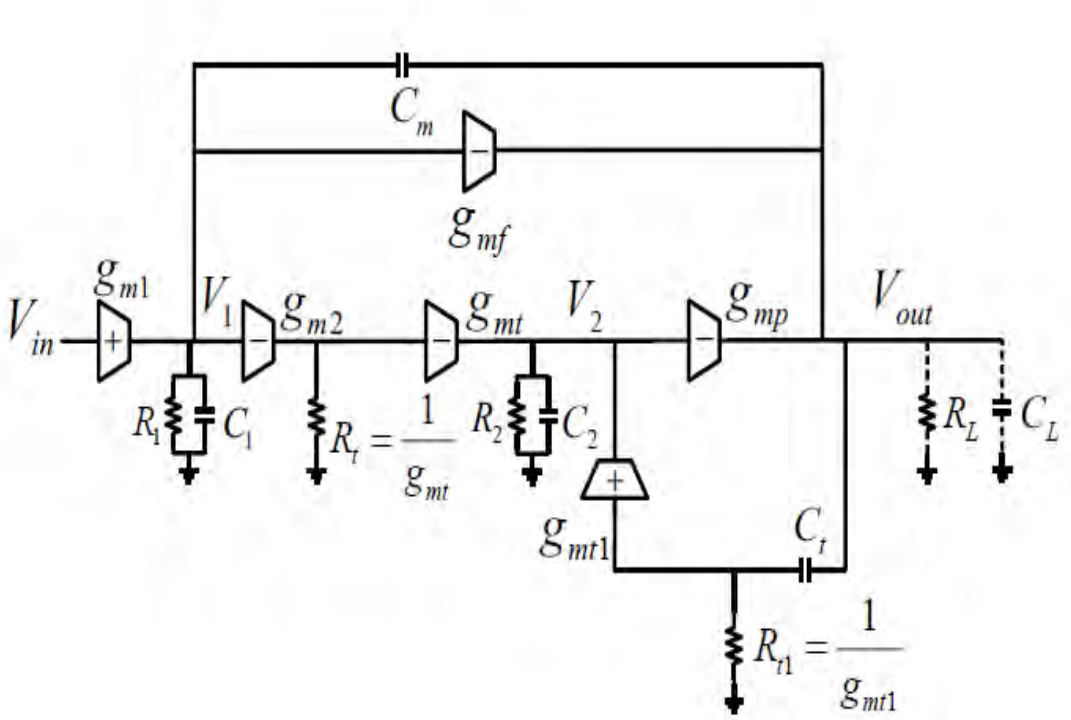

Figure 4.4: *Small signal simplified model*

Provided that the DC gain of every stage is sufficient and that for the first stage, the following statement is true. $C_m \gg C_1$. The load capacitance, denoted by C_L, is significantly higher than both C_m and C_t, which have much lower values.

$$gm_1R_1, gm_2R_2, gm_{pRL} \gg 1 \tag{4.7}$$

$$C_m \gg C1; C_m, C_t \ll C_L \tag{4.8}$$

It is pertinent to keep in mind that C_2 consists of the gate parasitic capacitance of the power MOSFET and is consequently quite big because of this. The following equation is the small-signal transfer function that was obtained regarding the open-loop gain of the output capacitor-less low-dropout (OCL-LDO) circuit:

$$A_v(s) \approx \frac{A_{dc}\left(1+s\frac{g_{m2}g_{m_p}C_t}{g_{m2}g_{m_p}g_{m_t1}}-s^2\frac{g_{m_t1}C_mC_t}{g_{m2}g_{m_p}g_{m_t1}}-s^3\frac{C_2C_mC_t}{g_{m2}g_{m_p}g_{m_t1}}\right)}{\left(1+\frac{s}{|p-3dB|}\right)} \times\left(1+s\frac{g_{m2}g_{m_p}C_t+g_{m_p}g_{m_t1}C_t}{g_{m2}g_{m_p}g_{m_t1}}+s^2g_{m_t1}C_2C_LR_L+\frac{C_2C_t}{g_{m2}g_{m_p}g_{m_t1}}R_L+s^3\frac{C_2C_tC_L}{g_{m2}g_{m_p}g_{m_t1}}\right) \tag{4.9}$$

The low-frequency gain, written as A_{dc}, and the dominating pole, denoted by $P-3db$, are defined as follows:

$$A_{dc} = g_{m1}g_{m2}g_{mp}R_1R_2R_L \tag{4.10}$$

$$p-3dB = -\frac{1}{g_{m2}g_{m_p}R_1R_2R_LC_m} \tag{4.11}$$

Thus, the Gain-Bandwidth Product (GBW) is:

$$\text{GBW} = \frac{g_{m1}}{C_m} \tag{4.12}$$

The resilience of the investigated LDO must be explored under varying loading scenarios, given that the load current may vary.

Case I (small output current): In this scenario, the equation $g_{m_t1}C_2C_LR_L \gg C_2C_t$ is true , suggesting a sizable difference across the two capacitance values if R_L is quite large.

$$p_1 = -\frac{g_{m_t1}\cdot g_{m2}}{g_{m2}+g_{m_t1}}\cdot C_t \tag{4.13}$$

$$p_2 = -\frac{(g_{m2}+g_{m_t1})\cdot g_{m_p}\cdot C_t}{g_{m_t1}}\cdot C_2C_L \tag{4.14}$$

$$p_3 = -\frac{g_{m_t1}}{C_t} \tag{4.15}$$

$$z_1 = -\frac{g_{m_t1}}{C_t} \tag{4.16}$$

$$z_2 = \frac{g_{m2} \cdot g_{m_p}}{g_{m_t1} \cdot C_m} \tag{4.17}$$

$$z_3 = -\frac{g_{m_t1}}{C_2} \tag{4.18}$$

It should become clear from the preceding information that p_3 and z_1 can nullify each other. $z_2$and z_3 are each of the two zeros, and they are only present at very high frequencies.

The optimal stability criteria for a third-order Butterworth frequency response having a damping factor of $\zeta = \frac{1}{2Q} = 0.707$ are as follows:

$$Q > \frac{1}{2} \tag{4.19}$$

By maintaining stability and good choices, these requirements provide the necessary damping for a third-order Butterworth filter.

$$p_2 = 2p_1 = 4\text{GBW} \tag{4.20}$$

Equation (15) is straightforward to satisfy $\frac{g_{m2}}{g_{m1}}$ and $\frac{g_{m_p}}{g_{m1}}$ are high. The lowest circuit stability happens when there is zero load current and the load capacitance is at its highest, because p_2 is proportional to g_{m_p} Since p_2 will be driven to increased frequency ranges as load current rises, phase margin will also grow.

Case II (current with modest to maximum output:) In this particular scenario, the load resistance $R_L$is quite low because it is highly influenced by the load current ($R_L \propto \frac{1}{I_{LOAD}}$). There is no change to the terms for the zeros, dominant pole, or GBW. Anyway, the non-dominant poles shift, as shown by the following:

$$p_1 = -\frac{g_{m_t1} \cdot g_{m2}}{g_{m2} + g_{m_t1} \cdot C_t} \tag{4.21}$$

$$p_2 = -\frac{(g_{m2} + g_{m_t1}) \cdot g_{m_p} \cdot R_L}{C_2} \tag{4.22}$$

$$p_3 = -\frac{1}{R_L C_L} \tag{4.23}$$

It is clear that p_1 is unchanged. Because GBW is independent of the present load, the relationship $p_1 = 2\text{GBW}$ remains valid. Since p_3 is positioned at a higher frequency than GBW when R_L is small, it does not affect LDO stability. As a result, the stability of the loop is conditional only on the position of p_2. The bigger g_{m_p} shifts p_2 to higher frequencies, enhancing the phase margin, despite the fact that $R_L$is smaller than in the previous instance. To boost the phase margin, the zero z_1 is placed somewhat beyond the gain bandwidth.

In reality, SRE makes the circuit more steady. Figure 2 is revisited in order to examine the second gain stage's real close transconductance g'_{m2} in greater depth. Since $R_t = \frac{1}{g_{m_t}}$ parallel r_{ds19}, we get $g'_{m2} = g_{m2}R_t \cdot (G_{m1} + g_{m_t})$. As soon as the SRE circuit has a failure and the overall system is subjected to a moderate level of load. , $g_{m2} < g'_{m2}$ which indicates that p_1 and p_2 come near to the UGBT and the stability of the circuit marginally worsens. When operating under high loads, the situation improves since p_2 is still driven to very high frequencies.

4.2 Circuit Realization and Schematic

Figure 5 illustrates the capacitor-less LDO schematic design using a high-slew rate (SR) error amplifier. Because it is possible to obtain a high output impedance and save more headroom than with a basic cascode amplifier, the single folded-cascode error amplifier design is frequently used for the first stage of the LDO error amplifier here, from M1 to M9. Transistors M10–M19 form a non-inverting amplifier in the second stage. A power transistor, known as Transistor Mpass, functions as an essential component in the push-pull output stage alongside the feed-forward transconductance unit M21. The capacitors C_m and C_t play a role as frequency compensation components. The symbols R_L and C_L denote the total output resistance of the low-dropout regulator (LDO) and the load capacitance, as mentioned earlier.Transistors M11, M14, M20, and M21 have transconductances ofg_{m_t}, $g_{m_{t1}}$, $g_{m_{t2}}$, and g_{m_f},respectively. The voltages V_{bn}, V_{bp}, and V_{cp} supplied by the bias circuit are the bias voltages. The design has a quiescent current consumption of 22 μA.

The slew rate must be determined using following ralation.

$$Slewrate = \frac{I_{b1}}{C_L} \tag{4.24}$$

The output current slew rate was configured to be 50 mA per microsecond, while the input voltage (VIN) was established at 1 volts.

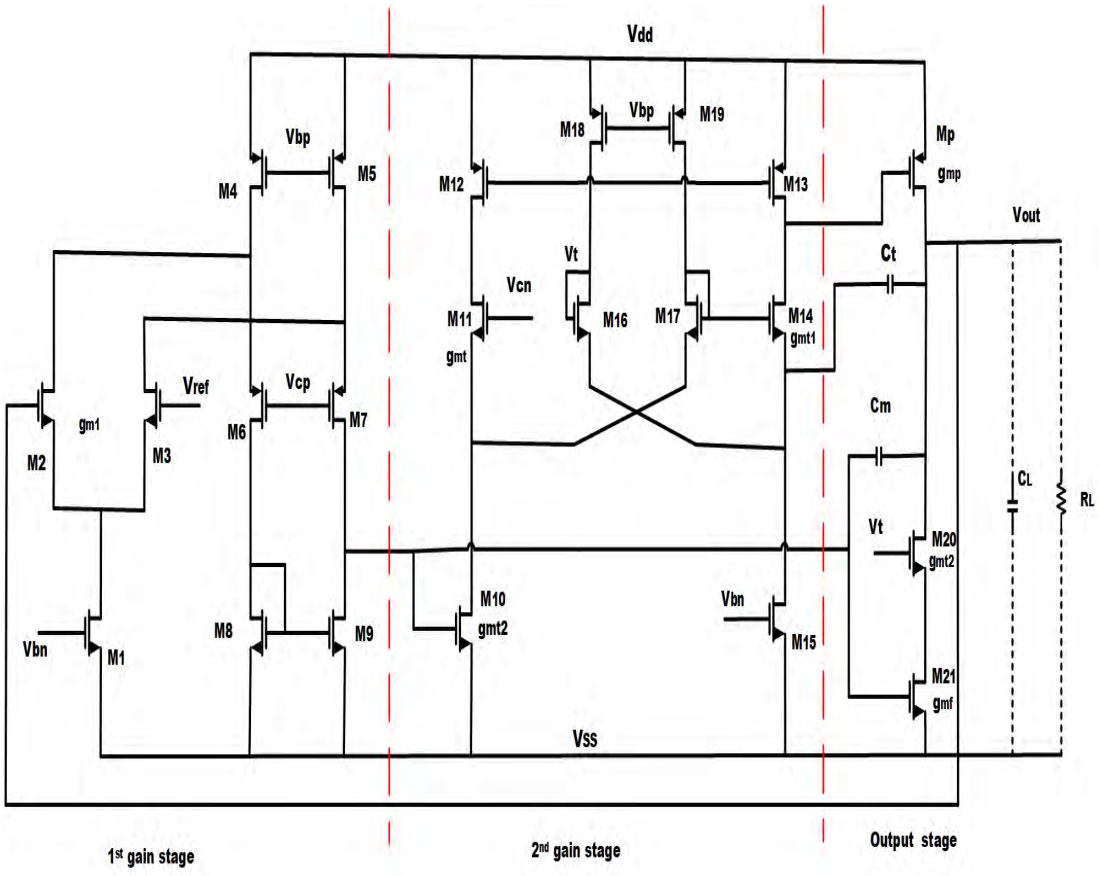

Figure 4.5: *Schematic diagram of the OCL-LDO circuit*

4.3 Reducing Overshoot and Undershoot

The rate of slewing at both the pmos gate node and the output node influences the circuit's response to spikes. Two charging and discharging routes are shown in Figure 4.5; one uses transistors Mp, M20, and M21, while the alternate route uses M13 and M14. Three current mirrors are needed to build

Table 4.1: Designed Circuit Parameters

Transistor	**Widthμm**	**Lengthμm**
M1	8	1
M2, M3	10	1
M4,M5	9	1
M6,M7	9	1
M8,M9	9	1
M10,M15	5	1
M11,M14	6.66	1
M12,M13	10	1
M16,M17	1	1
M18,M19	12.5	1
M20	55	1
M21	50	1
Mp	2m	1

the push-pull output stage, which provides the amplifier with a bit of sink and source output driving capability. In order to optimize the transitory response, it is imperative to dynamically supplement the current within these crucial pathways. Another sensing network is utilized for the purpose of detecting output voltage surges and enhancing the slew rate. The coupling interaction between C_m and C_t is employed for the purpose of catching load current switching requests, monitoring variations in V_{out}, and transmitting this data to a pair of current boosters, which are comprised of M14 and M20. These boosters facilitate the C_L and C_{GD} of MP to get charged and discharged instantly.

As the output voltage, V_{out},leads to a sharp surge , ΔV, as a reaction to a high-priority load current request, the capacitor, C_m, detects the spike and modifies the gate voltage of transistor M14 by a negative value of ΔV using an inverter circuit made up of transistors M10 and M17. Concurrently, the voltage originating from its source undergoes a change denoted as ΔV as a result of the coupling effect of C_t, leading to a corresponding alteration in V_{GS} in M14 by a factor of $-2 \cdot \Delta V$.

In instances where V_{out} experiences undershoot, the current flowing down via M14 is amplified, while the current flowing through M13 is diminished due

to the duplication of the current mirror established by M12 and M13. Thus allowing the second stage to increase its current draw in order to discharge the parasitic capacitance of the gate of transistor Mp. On the contrary, in the event of V_{out} overshooting, the circuit exhibits a behavior that is contrary to its normal operation as it rapidly charges the gate capacitance of transistor Mp.

The enhancement of the slew rate is achieved by the push-pull final output stage consisting of M21 and Mp for the output node. Significantly, the trajectory established by M20 and M21 serves as the principal route for dissipating surplus current in instances where V_{out} experiences overshoot. Therefore, although it is vital to decrease the current of Mp, it is of greater significance to enhance the current flowing via M20 and M21 in order to mitigate the overshoot of V_{out}. Thankfully, M20 can do so by drawing a substantial current, just as M14. To preserve power, the dynamic current boost process is turned off when V_{out} stabilizes.

4.4 Experimental Results and Discussion

The studied capacitor-less LDO is a conventional 55nm CMOS implementation that, when fed an input voltage greater than 0.7V, generates a 0.8V voltage as the output at a 10mA output current ,illustrated in fig 4.6.

In this study, the transient load response , which is primarily dictated by the slew rate (SR) and bandwidth of the low-dropout regulator (LDO), is assessed by simulation in order to evaluate its transient performance.Fig 4.7 shows the output voltage V_{out}= 0.8V of the designed circuit and I_{load}= 1 mA.

The findings indicate that the complete restoration of the output voltage can be achieved in a time frame of 0.4 μ s when subjected to a voltage spike of less than 40 millivolts.. An instance of significant undershoot at the output is observed when there is a transition in load current from low to heavy load.

Figure 4.6 demonstrates that the utilization of the SRE circuit in the LDO results in notable enhancements in transient responses under low-power conditions. This improvement is achieved with a mere 29.4 percent increase in static current consumption.

The phase and the gain margin are displayed in Fig. 4.8. It shows that

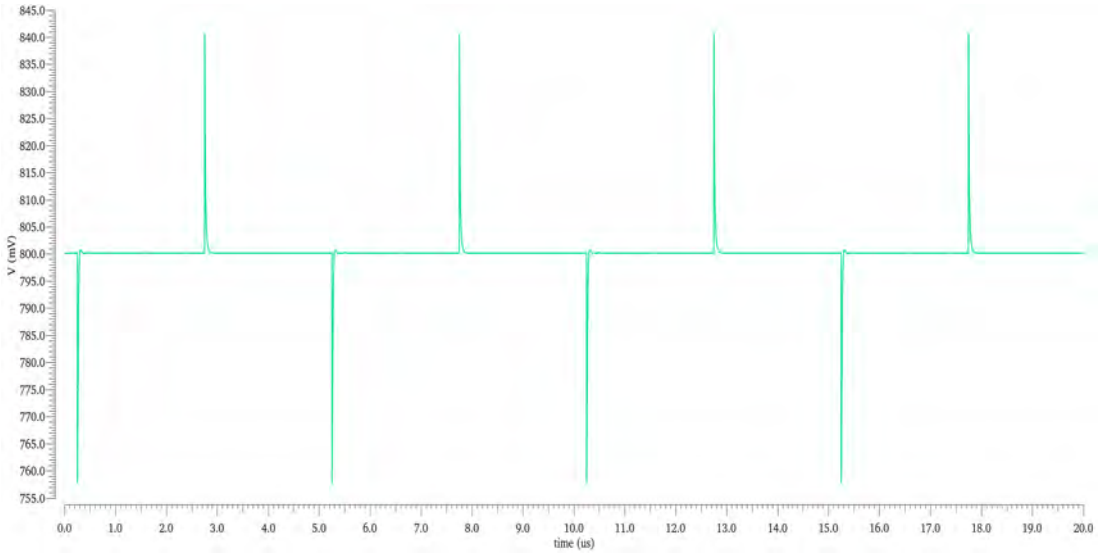

Figure 4.6: *Measured Output Voltage 0.8V for Vin=1V and CL=0 F*

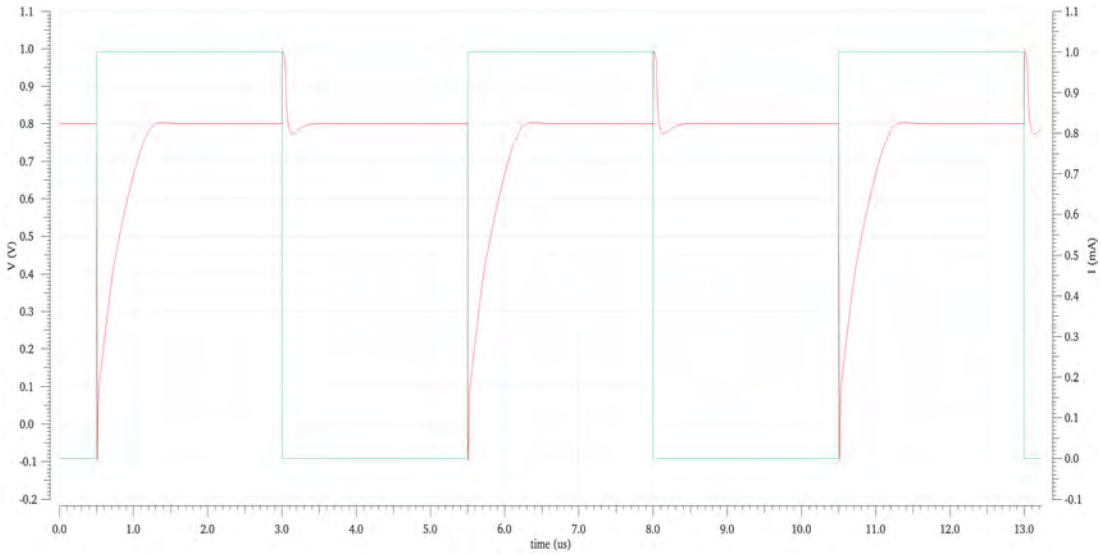

Figure 4.7: *Results from transient simulations for IL=1mA with CL=0 pF*

at no-load condition the phase margin and the gain margin of the Error-amp are around 102◦ and 94dB, respectively.The phase margin, however, shrinks with increasing load due to the three-stage operation. Because the dominant and non-dominant low-frequency poles are closer together at minimum load current state, this is typically where worst-case scenarios for LDO (two-stage)

exists.The GBW product is 34.74 MHz.

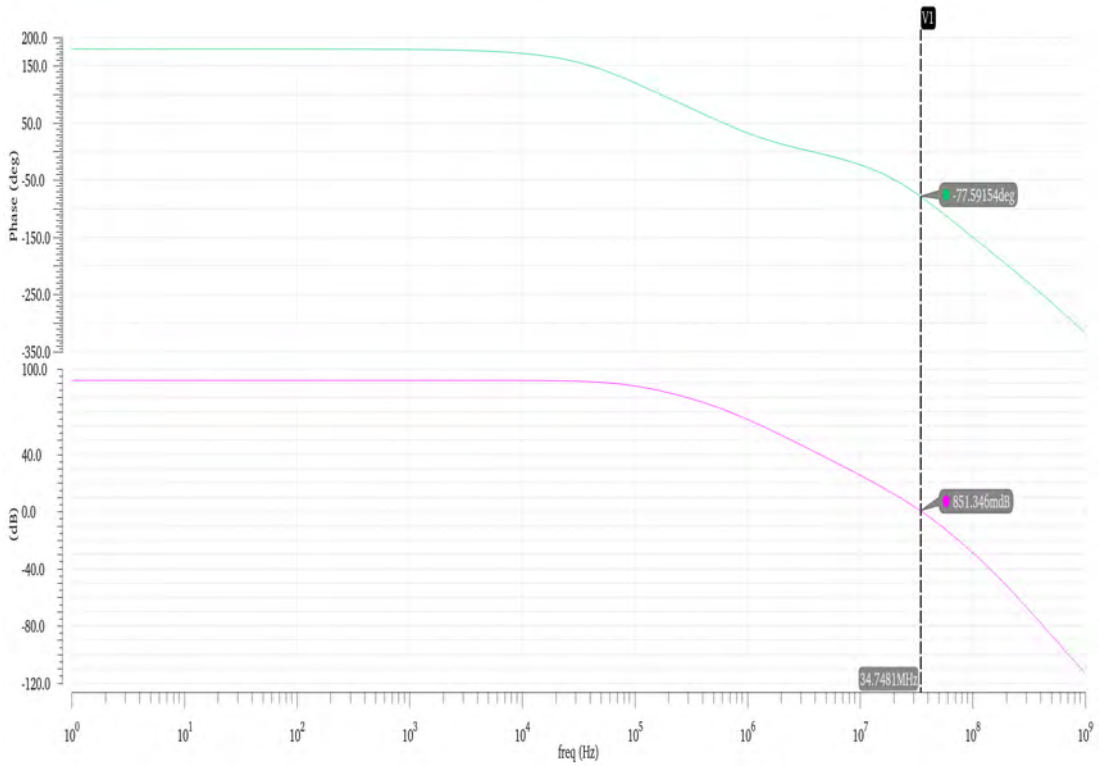

Figure 4.8: *Simulated Loop Gain of the Regulator*

The line-transient is recreated to show that the SRE circuit really isn't prone to changes in the supply voltage. Figure 4.9 illustrates the transient response of the system, specifically focusing on the behavior of a 1pF on-chip output capacitor. The input voltage (VIN) ranges from 0.8V to 2.4V. The absence of dynamic flares and introduced noise ensures the circuit operates with robustness.

The low-dropout (LDO) regulator demonstrates a strong static line regulation due to the significant voltage gain offered by the folded-cascode amplifier.

The load regulation response of the regulator is depicted in Fig 4.10, illustrating the change in load current from 0 mA to 50 mA.

It is worth noting that in the three-stage configuration, the regulator demonstrates a more precise match to the desired output voltage due to its larger open-loop gain.A listing of regulator design outcomes is provided in Table 4.2.

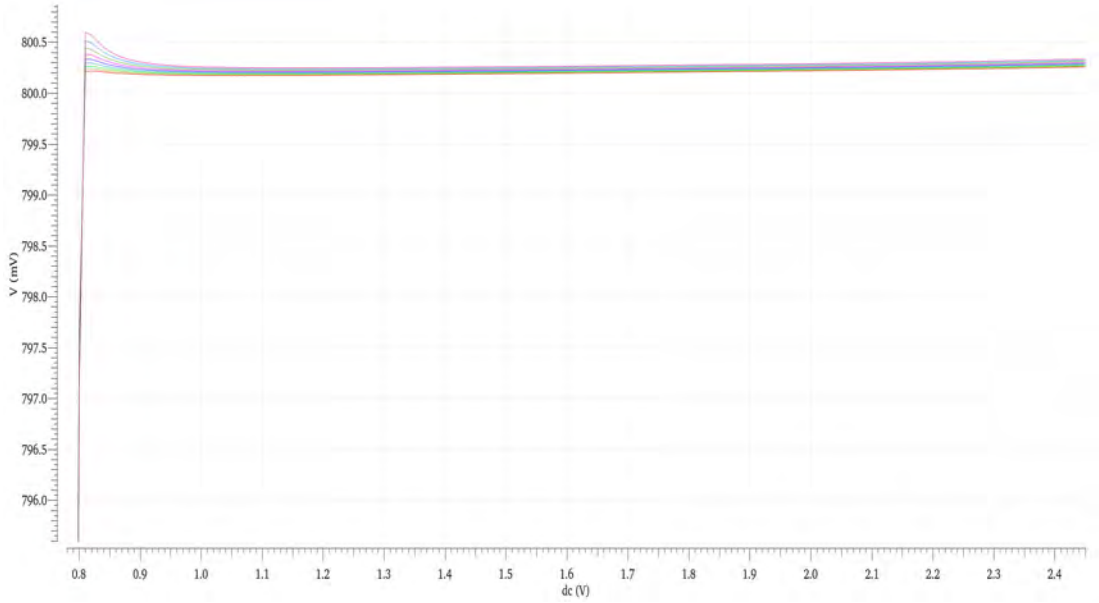

Figure 4.9: *The simulation findings for line regulation for IL=1 mA and CL=0 F*

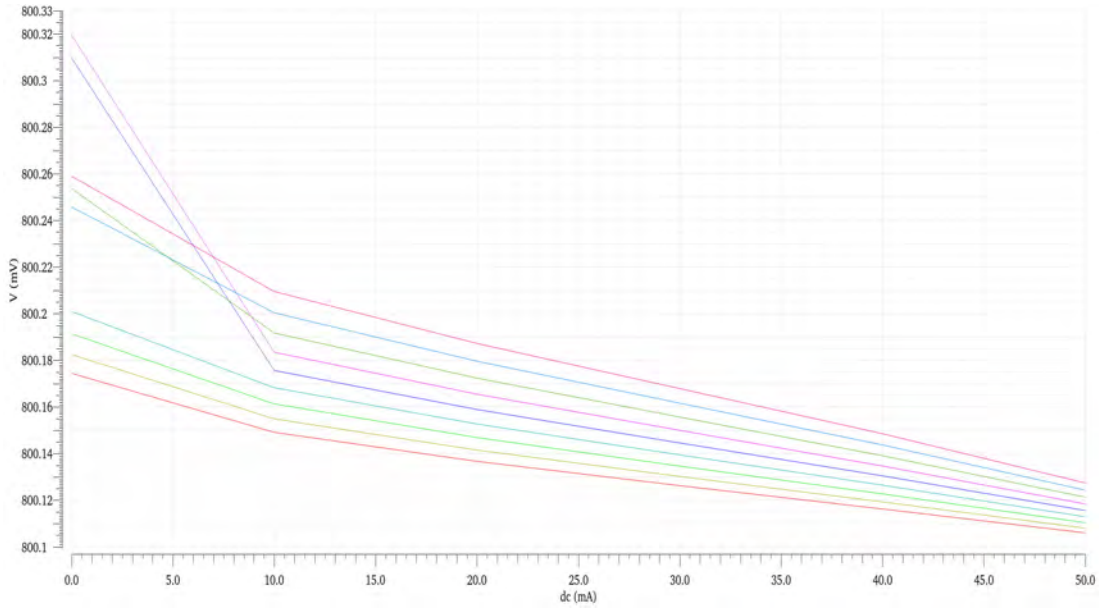

Figure 4.10: *The Simulation Outcomes of Load Regulation for Vin=1V and CL=0 F at the temperature variation from -40° to 120°C*

Table 4.2: Summary of the Measured Results

Parameter	Specification	Measurement	Units
Input Voltage	0.8-2.4	0.8-2.4	V
Max. Load Current	50	50	mA
Output Voltage	0.8	0.8	V
Recovery Time	< 400	400	ns
US, OS	< 40	37.5	mV
Quiescent Current	3	1.04	%
Load Regulation	10	8.3	mV/mA
Line Regulation	1.2	0.151	mV/V

4.5 Comparison

Table 4.3 demonstrates a comparison in efficiency of the implemented LDO with various previous capacitor-less LDO designs, giving a clear image of the performance improvement. The suggested LDO design has various applications in battery-powered systems due to its effectiveness as a heavy-load regulator. The 8.3 μ V/mA DC load regulation is achieved while maintaining a reasonable DC loop gain, making it one of the reasonable load capabilities among the compared LDOs. Achieving appropriate load regulation with a high load current is challenging because, in the majority of LDO designs, the loop gain of the LDO decreases with increasing load current.Ultimately, a Figure of merit is selected as a benchmark for evaluation and comparison.The good FoM factor achieved in this research makes it an attractive option for use in portable setups that rely on batteries.

$$FoM = K\frac{\Delta V_{out} * I_Q}{\Delta I_{LOAD}} \tag{4.24}$$

$$K = \frac{\Delta t \text{ used in the measurement}}{\text{the smallest } \Delta t \text{ among designs for comparison}} \tag{4.25}$$

K must be calculated by the ratio of the measurement's change (Δt used) to the smallest change among the designs being compared ($\Delta$for comparison).

Table 4.3: FoM Performance Comparison with previous work [1, 2]

Parameters	**TPEL[17]**	**TPEL[21]**	**This Work**
Year	2020	2022	2023
Technology	65nm	0.35μm	55nm
V_{DO}(mV)	150	200	200
V_{out}(V)	0.8	2.5	0.8
$I_{LOAD(max)}$(mA)	100	100	50
$I_{LOAD(min)}$(mA)	0	0.01	0
$C_{on-chip}$(pF)	6	14	2
C_L(pF)	0-100	0-100	0-100
I_Q(μA)	14	66	22
ΔV_{out}(mV)	230	255	37.5
ΔI_{LOAD}(mA)	100	100	50
Line Reg.(mV/V)	12	0.8	0.312
Load Reg.(μV/mA)	90	60	213
Settling Time (μs)	1.2	0.7	0.4
FOM (μV)	70.84	673.20	12.84

4.6 Layout

Figure 4.11 shows the die diagram. The total die size is 45μm x 532 μm. This chip has employed 55 nm CMOS process.

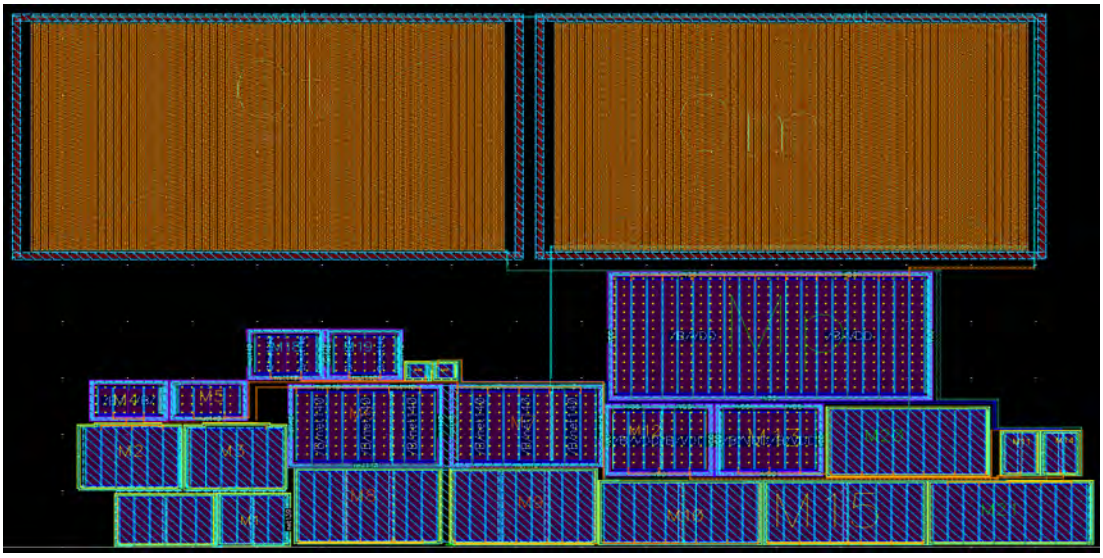

Figure 4.11: *Layout of LDO with slew rate enhancement*

Chapter 5

Conclusion

This thesis studies two prototype designs of fast-transient capacitor-less low-dropout (LDO) regulators, implemented using 55nm CMOS technology. These regulators quickly respond to load current changes, reducing power supply noise. The initial design avoids the need for a large off-chip capacitor, following a common LDO design trend. The focus then shifts to enhancing transient response characteristics.

The LDO_1 circuit is augmented with a transient response enhancement module that operates on the principle of slew rate enhancement. In order to achieve improved line regulation and load regulation performance, it is necessary to maintain a large DC loop gain ($\gg 60dB$) throughout various load circumstances, without employing the adaptive bias approach for error amplifier DC bias changing. It enhances the CL-LDO's overall transient response. The provided input voltage is 3 volts, whereas the output voltage is measured at 1.2 volts. As the variation in load occurs from 0 to 50 mA in a time period of 1 μs, the output of the CL-LDO exhibits an overshoot voltage of 0.15 V, an undershoot voltage of 0.17 V, and a recovery time of 0.1 μs. The quiescent current was limited to 59 μA. The LDO is capable of delivering 1 mA of output current with a dropout of 200 mV while consuming only 1 mW of power.

The second LDO design features a high-slew-rate amplifier, low quiescent current, and a large pass transistor to enhance transient response. It employs low-power capacitive coupling to improve the error amplifier. This reduces gate capacitance charging time, enhancing load and line transient responses

and reducing power supply noise. The experimental findings demonstrate that,with the addition of Slew rate Enhancement circuit, the studied LDO_2 regulator, which has an I_Q of just 22 uA, provided a supply voltage of 1V exhibits an OS of 40mV and US of 35mV with the recovery time of 0.4μs in the most unfavourable conditions. The second LDO, powered at 1V with 71μW power consumption, exhibits minimal overshoot and undershoot (well below 200mV) when the load current jumps from 10mA to 50mA in just 1μs. It successfully achieves the desired output voltage of 0.8V.

The study validates the LDO regulator's stability without the need for on-chip or off-chip capacitors, ensuring a reasonable transient response with minimal overshoot and undershoot. Both designed LDOs meet specified requirements, demonstrating the potential to create high-performance LDOs with minimal quiescent current. These low-power LDOs can extend battery life in various mobile devices, assessed using a figure of merit (FoM).

$$FoM = T_s \frac{I_q}{I_{load(max)}} \tag{5.1}$$

Table 5.1: FoM Comparison [3, 4]

	[3]	**[4]**	**This Work**
FoM[ns]	0.0324	0.067	0.0176

The variable "T_S" represents the settling time of the output voltage. The settling period of the output voltage is discussed in references [13] and [16].

The integrated LDO's FoM was calculated like [13] and [16], using T_S as settling time within 5 percent of nominal output voltage. It's slightly higher due to the compensation components, but the LDO meets strict standards and is on par with Table 12 designs

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