LDO DESIGN FOR WEARABLE SYSTEMS IN NANOMETER CMOS TECHNOLOGY

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Certificate

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Alveena Siddique

Dedication

"In the name of Allah, the Most Gracious, the Most Merciful"

I Dedicated This Dissertation To

My beloved Father, Brothers, and my Mother

Abstract

In modern electronics, two key priorities stand out: maximizing battery life and optimizing chip space utilization. Low dropout regulators (LDOs) play a crucial role in enhancing the performance of wearable devices by extending battery longevity. The conventional LDO design typically requires large external capacitors, it consumes considerable die area. To reduce the area, an innovative capacitor-less LDO is used. This thesis study two capacitor-less LDO design as the transistor level simulation in SMIC 55nm CMOS Technology. The first ldo design integrates a comparator circuit, to improve transient response. It has a input voltage range of 0.8-V to 2.4-V and maintains output almost 0.8-V over load from 0 to 50-mA with power consumption of 90μW. The circuit output ripple is below 40-mV. The settling time of 0.2μs and a quiescent current of 26μA at maximum load. The second capacitor-less LDO circuit utilizes a folded cascode amplifier, it can achieve settling time reduction twice of the first design. It remains stable without an output capacitor throughout a complete load range of 0.1-mA to 50-mA. The output voltage recovers within 0.1μs with a voltage ripple of less than 100-mV with power consumption of 62μW. The circuit has a quiescent current of 22μA, and a 200mV dropout voltage at 0.8 to 2V. It regulates the circuit output voltage to 0.6-V. Both LDOs offer efficient load and line transient responses, reduced settling times, and resilience to process, voltage, and temperature variations, ensuring consistent and reliable performance.

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Chapter 1

Introduction

1.1 Overview

The demand for power management ICs (PMICs) is increasing rapidly due to the wide range of applications that need varying supply voltages. These applications include mobile devices [1], automotive systems [2], Internet of Things (IoT) hardware [3], and wearables [4]. In order to fine-tune DC voltage levels, voltage regulators, also known as switching regulators, are often used. This includes boost converters designed for particular uses, such as LED drivers. It is essential to use switching converters and low dropout linear regulators (LDOs) in order to provide the delivery of accurate voltage while maintaining high efficiency and a low quiescent current. The semiconductor and consumer electronics industries are now focused on two significant trends: chip size reduction and power consumption minimization. As a result, integrated electronic systems have been designed to efficiently manage voltage levels and determine whether power and voltage converters should be integrated on the chip or off the chip. The specifications of the voltage subdomain should be taken into consideration while deciding between linear and switched circuits. In devices like smartphones, tablets, or wearable gadgets, various components such as microprocessors, sensors, displays, and memory chips require different voltage levels to operate efficiently [7]. LDO regulators step-down higher input voltages (typically from a battery or external power source) to lower, stable output voltages required by these components. In order to fulfill the need for more compact, energy-efficient devices with longer battery lives, especially for use in wearable devices, it is crucial to design reg-

ulation systems with frequency compensation mechanisms and appropriate feedback networks to ensure stability.

A power management unit is often made up of numerous components, comprising switching regulators like buck converters, boost converters, and linear regulators, as shown in Figure 1.1.

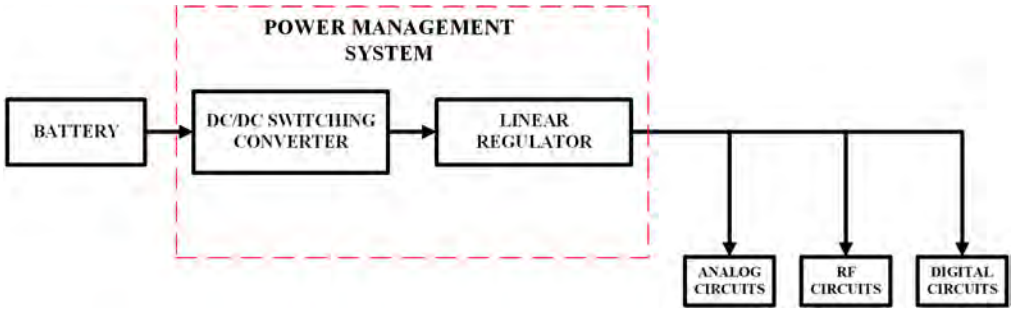

Figure 1.1: Power Management System

This thesis emphasizes the design of an efficient power source for wearable applications, with the goal of achieving a system-on-chip (SoC) solution with the intention of integrating the voltage regulator core along with the extra circuitry that is required on a single chip, hence eliminating the usage of external components. CMOS technology adoption is the most cost-effective choice in this context.

1.2 Design Considerations

An LDO is a type of voltage regulator commonly used in wearable devices to provide stable voltage to the system despite fluctuations in the input voltage or changes in the load. Many aspects must be addressed while developing a voltage regulator. Minimizing power usage is always important, especially with wearable consumer devices [5]. The regulator's power consumption may be reduced by lowering the dropout voltage. A device with lower power consumption may use a smaller battery, resulting in enhanced portability [6]. The bandwidth of the voltage regulator is another key feature to consider while designing it. A regulator's ability to maintain a constant output voltage and respond swiftly to changes in the input and power supply is directly

proportional to the bandwidth of the regulator. An additional benefit of a regulator with a high bandwidth is an improved power supply rejection ratio (PSRR), a metric for the regulator's ability to significantly reduce power supply noise. A higher power supply rejection ratio results in a smaller variation in the output voltage when there are variations in the supply. Stability is yet another aspect that must be taken into consideration while designing voltage regulators. It is not ideal to have a voltage regulator that is prone to oscillation since the function of a voltage regulator is to offer other components with a constant voltage. The stability of the system is dependent on the load circumstances, which include the output current and the load capacitance. Load regulation refers to the amount of change in output voltage that occurs when there is a change in the output current. This is closely linked to stability. The significance of the various voltage regulator requirements varies greatly depending on the specific application. Power efficiency is key for wearable devices devices that run on batteries as opposed to stationary ones that plug into an outlet.

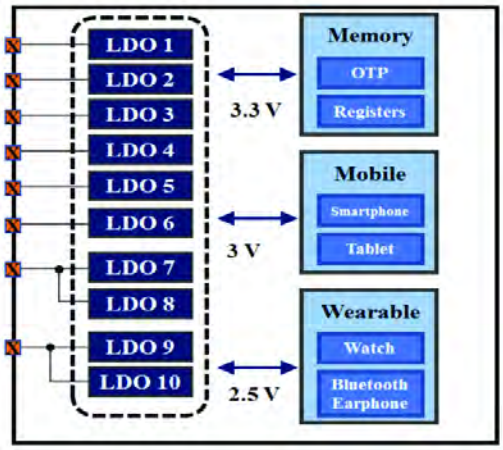

Figure 1.2: LDO's Applications

1.3 Switching Regulators / DC-DC Converter

Switching regulators are used when there are big differences in voltages between the input and output or when a lot of current needs to flow through a load. Switching regulators may provide output voltages that are greater than the input or have the opposite polarity, something a linear design cannot do. Unlike linear regulators, they often need external components such as an inductor or capacitor to serve as an energy storage element. An input DC voltage is changed by a switching regulator into a high frequency voltage. The AC voltage is then filtered, and the filtered DC voltage is sent back to the input. To achieve the first DC to AC conversion, a switch (typically a transistor) that connects the unregulated input voltage to a storage element (commonly an inductor) is quickly switched on and off. As a result, there is an AC ripple at the storage element's output. This may be low-pass filtered, commonly using an LC network, to create a DC voltage at the output. In essence, DC-DC converters may be categorized into two types: In Buck mode, the output voltage is less than the input voltage; in Boost mode, the reverse is true. Figure 1.3 displays the configuration of the two converters.

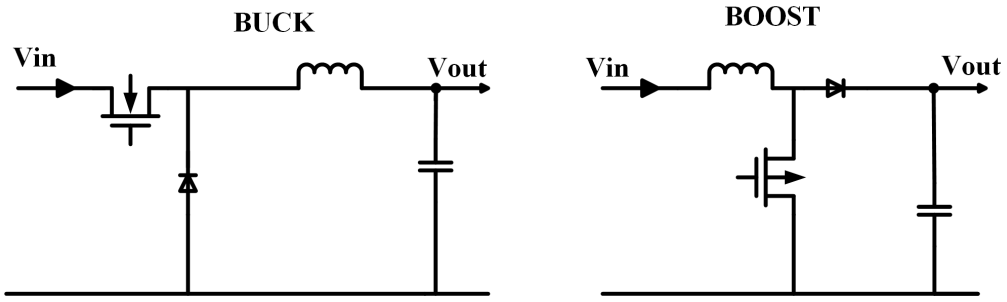

Figure 1.3: Buck and Boost Converter Topologies

The primary issue associated with not exclusively using the DC-DC converter primarily the presence of fluctuation in the output voltage, often referred to as ripple. To reduce the ripple and load fluctuations, a LDO is used after to the DC-DC converter. The DC-DC regulator is specifically designed to reduce the drop in voltage across a linear regulator under loading situations, as shown in Figure 1.4.

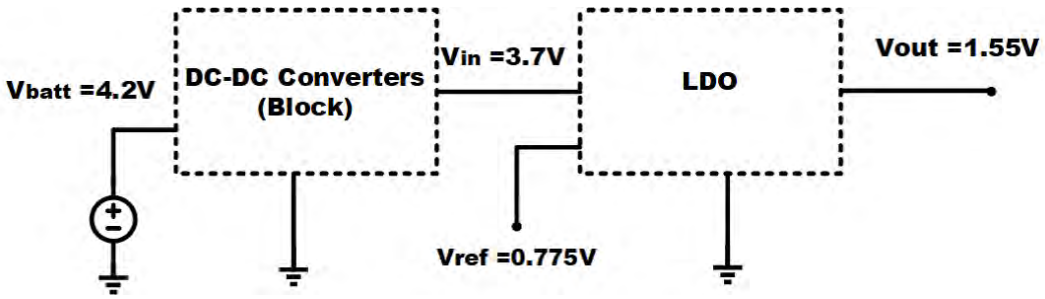

Figure 1.4: Ideal Linear Efficiency Regulation

1.4 Linear Regulator

The linear regulation of the output voltage has many benefits, including improved power supply rejection, reduced output noise, and enhanced dynamic response. Two of the most significant limitations are limited to down conversion and low efficiency. Considering that the power efficiency of linear regulators is inversely proportional to the voltage drop across the control device, changes in the DC input voltage have a significant impact on the efficiency of the regulators' power consumption. A regulator is considered to be less efficient when there is a greater disparity between the input and the output. A higher current load also results in a higher power loss. Hence, linear regulators may not be appropriate for some systems that need large current loads.

$$P_{dissipation} = (V_{in} * V_{Out}).I_{load} \tag{1.1}$$

It is common practice to include a switching regulator prior to the linear regulator in order to enhance overall efficiency in cases when the input voltage exceeds the restricted output. As depicted in the Figure 1.5, the linear regulator is a DC-DC voltage converter that regulates the input DC voltage linearly to produce a lower output DC voltage.

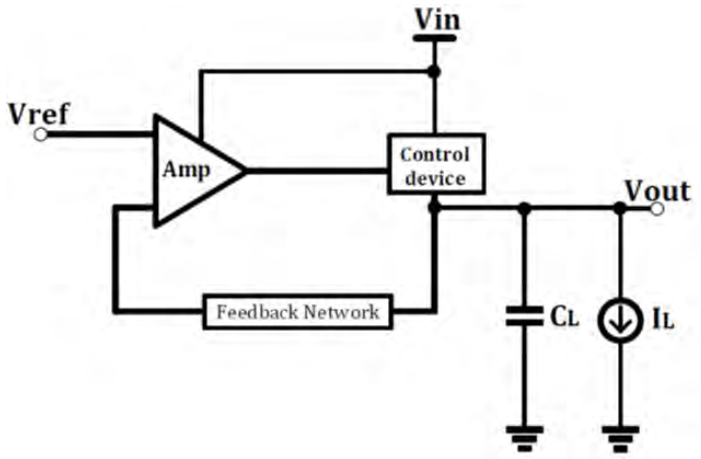

Figure 1.5: Linear Regulator

A power transistor's orientation is the only thing that makes these two designs different from each other. Conventional linear regulator employs a transistor coupled in a common drain arrangement. Alternatively, this transistor may be substituted with a BJT transistor or two transistors arranged. In contrast, LDO regulators employ common source configuration. The orientation of a power transistor has a direct correlation with both the mode of operation and the stability of the linear regulator.

1.5 LDO Regulators

Negative feedback system for producing a clean constant output voltage, as illustrated in Figure 1.6. The pass element regulates the output voltage by reducing the current supplied to the output, hence causing a decrease in the output voltage while maintaining a constant level.

LDO voltage regulators are widely utilized in design due to their excellent performance, cost effectiveness, and simplicity. The voltage drop that occurs across the power mosfet is the mode of operation that the regulator will use. When it comes to the functioning of a linear regulator, there are three distinct regions that may be distinguished from one another: the dropout region, the linear region, and the off region.

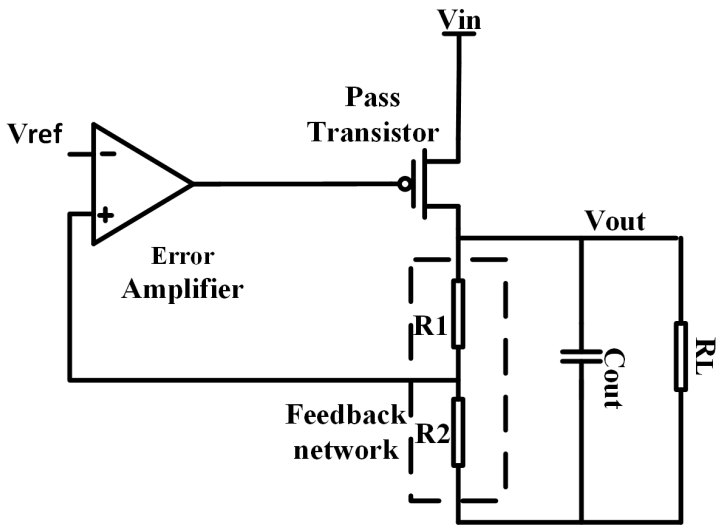

Figure 1.6: LDO Regulator

•Linear Region:
The output voltage level is sufficiently high for the LDO regulator to function properly, ensuring the stability of the output voltage and providing the necessary current to the load.

•Dropout Region:
As one or more transistors approach the triode area, the input power is decreased, causing the control loop to lose gain and the LDO regulator to be unable to regulate any more.

•OFF Region:
The power supply voltage is insufficient to maintain all the transistors turned on, therefore the circuit is switched off.

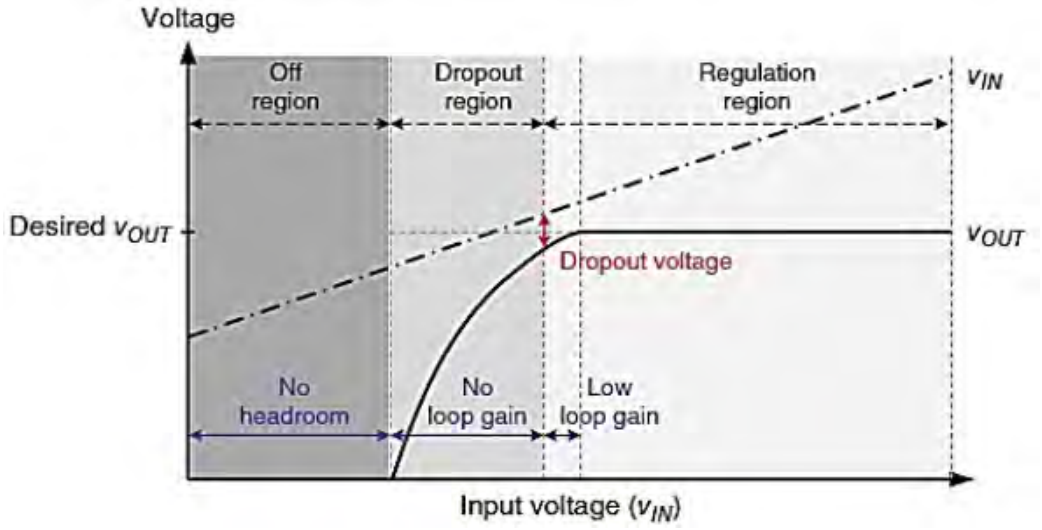

Figure 1.7: LDO voltage regulator input-output voltage characteristics

LDO voltage regulators are significant because of their ability to address voltage control challenges in a variety of applications. Unlike other voltage regulators, such as switching regulators and low dropout regulators operate in a linear mode. Cap-less LDOs, which do not need discrete components, and their smaller size contribute to their lower cost compared to switching regulators. For these reasons, LDO is the most suitable choice for integrating into implanted biomedical electronics to provide controlled power.

1.6 Building Blocks of LDO Regulator

The basic components of an LDO regulator are:
1. Error Amplifier
2. Pass Transistor
3. Reference voltage
4. Network Resistivity Feedback

1.6.1 Error Amplifier

The error amplifier (EA) performs a comparison between the reference voltage and the feedback voltage obtained from the output, and then amplifies the resulting difference. Its function is to drive the pass device's gate to the proper operating point to guarantee that the output voltage is accurate. In order to maintain a constant output voltage, the EA operates the pass device despite variations in the current load and power supply. Hence, the design of the error amplifier is vital in order to meet the driving specifications of the pass device and optimize the system's performance.

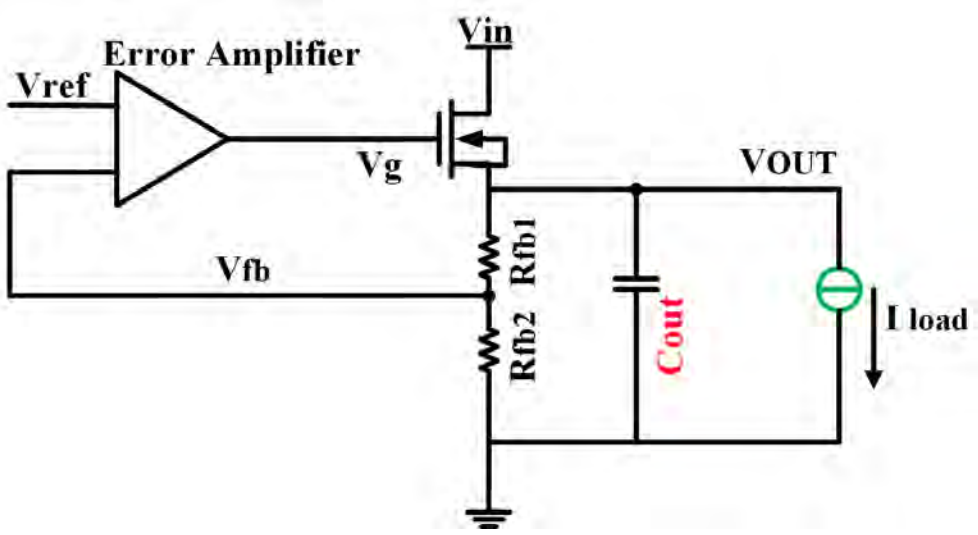

Figure 1.8: PMOS based LDO

1.6.2 Pass Transistor

In linear regulators, the output stage may be designed with a variety of various configurations which are determined by the performance of the circuit and the power efficiency of the regulator. An essential factor in the selection of the pass device is the dropout voltage, which refers to the difference between the input and output voltages. Typically, the nMOS transistor has more current conduction capability compared to transistors of the same size,

owing to its increased electron mobility. Nevertheless, to get a low dropout voltage, pMOS transistors are favoured, in spite of their poor current conduction capability. Furthermore, the gate voltage consistently remains below the supply voltage. with contrast, with nMOS, the gate voltage may exceed the supply voltage when it is specifically designed to function with a low dropout voltage. As a result, extra circuitry that adds to the design complexity may be necessary. Nevertheless, the nMOS transistor has less area in comparison to conventional transistors, although it has the capability to manage the same maximum current. Furthermore, it provides exceptional dynamic performance in situations involving large signals because of the direct linkage between the source node and the regulator's output. Hence, when the load current quickly changes, e.g. I_{Lmin} to I_{Lmax}, Vout decreases, and so V_{gs} quickly increases, thus regulating the pass device to drive I_{Lmax}.

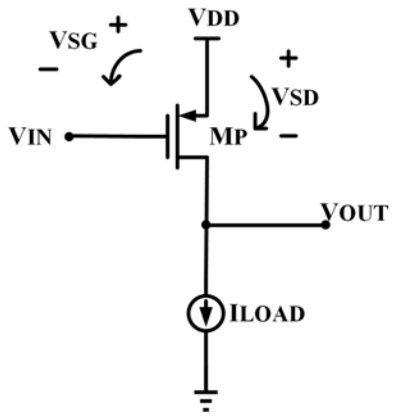

Figure 1.9: Pass Transistor

1.6.3 Reference Voltage

The voltage reference is required by the error amplifier in the LDO to compare and regulate the output voltage. Bandgap circuits are the main source of voltage references. Bandgap circuits use the complementary characteristics of semiconductor materials to provide a voltage that remains relatively stable even when temperatures fluctuate. However, it is important to note that the

current investigation did not utilize or construct a bandgap circuit. As a benchmark, a fixed direct current (DC) source was employed.

1.6.4 Feedback Network

The resistive divider typically consists of a pair of resistors connected in series and connected to the output. In certain ways, it level shifts the output voltage and produces a voltage that may be compared to the voltage reference at the error amplifier's inputs. The utilization of the resistive network divider enables exceptional precision and durability. To begin with, manufacturing variations is negatively correlated with resistor size. Furthermore, resistors exhibit reduced fluctuations in temperature. The feedback factor has a direct impact on the loop gain, and it is preferable to have a greater value in order to achieve effective rejection of power supply noise. The majority of designs often use a feedback factor of 0.5, especially when the two resistors are of similar value.

1.7 Working Principle of LDO

The output voltage ought to remain steady regardless of the load or supply change. When the load is activated, the gate voltage of the pass transistor adjusts via a negative feedback loop, enabling the pass transistor to provide the required load current. Similarly, when the load is off, the pass transistor enters the cutoff (sub-threshold) region and consumes a minimal amount of current to sustain a regulated output voltage, as seen in Figure 1.10 (a),(b) and (c). At the beginning, the output voltage was biased to position 1, as illustrated in Figure 1.10 (a) and (b). Suddenly, the current flowing through the load rises from I_{OUT1} to I_{OUT2}, causing a shift in the output voltage.

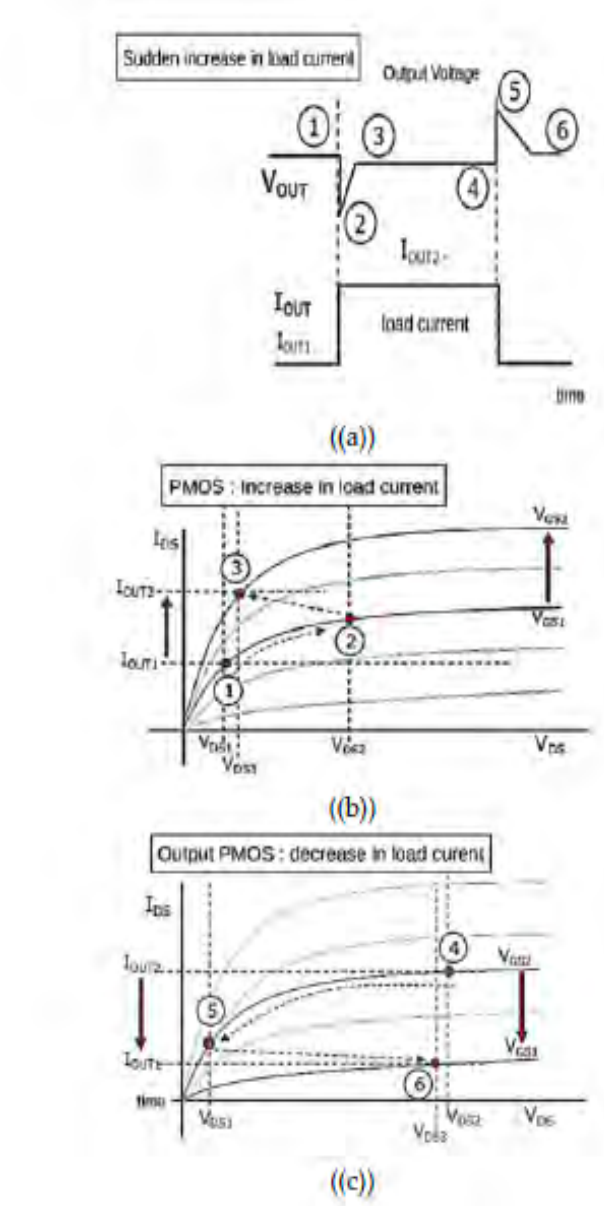

Figure 1.10: LDO working (a), (b), (c)

1.8 LDO Linear Regulator Characterization

The traditional approach to describing an LDO involves discussing its characteristics.

1.8.1 Static State Specifications

The static state characteristics comprise line and load regulation, as well as temperature coefficient effects. Typically, the performance of an LDO regulator in regulating the steady state output voltage for specified line and load steady state values is quantified by its line and load regulation specifications. The temperature coefficient determines how well the error amplifier offset voltage and voltage reference operate in tandem. Every steady state or DC requirement is illustrated in Figure 1.11, which functions as a benchmark.

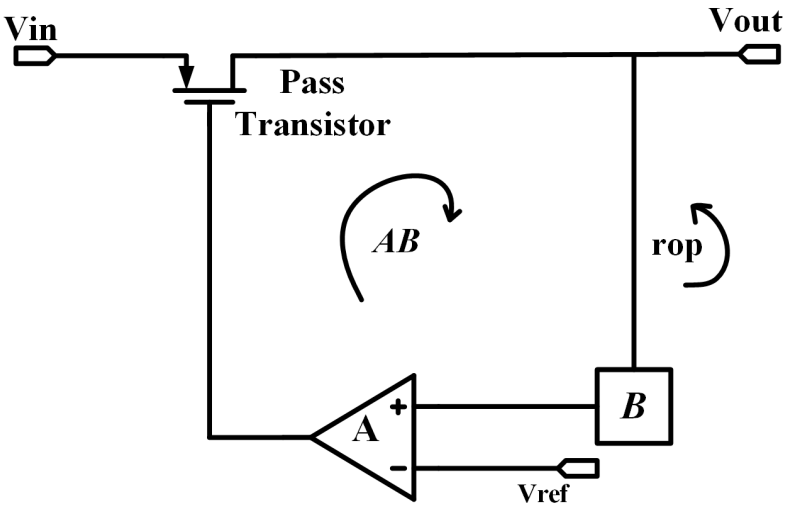

Figure 1.11: Closed Loop system

•**Line regulation**: Line regulation refers to the power supply's capacity to maintain the designated output voltage, even when there are fluctuations in the input line voltage. The quantity represents the discrepancy after the regulator has achieved a stable condition. Equation 1.2 provides a generic equation for line regulation.

$$\frac{\Delta V_{out}}{\Delta V_{in}} \approx (\frac{g_{mp}.r_{op}}{A\beta}) + \frac{1}{\beta}(\frac{\Delta V_{ref}}{\Delta V_{in}}) \tag{1.2}$$

Line regulation is contingent upon many factors, including the transconductance of the pass transistor g_{mp}, the output resistance of the low dropout

regulator r_{op}, the loop gain of the LDO, and the feedback gain. To enhance the line regulation, it is necessary for the LDO regulator to possess a loop gain that is suitably large. These amounts become obvious during the LDO regulator design debate.

•**Load regulation:** Load regulation refers to the amount of fluctuation in the output voltage when there is no load or when the load is at its maximum, while keeping the input voltage constant. The load regulation is determined by the product of the loop gain, and the output impedance of the pass transistor, r_{op}. The given relationship is expressed in Equation 1.3.

$$Load_{Reg} = \frac{\Delta V_{out}}{\Delta I_{out}} = \frac{V_{op}}{1 + A\beta} \tag{1.3}$$

For an LDO with an infinite open-loop gain, the load regulation would be close to zero. Additionally, load regulation is enhanced when the pass device's output impedance is reduced. The load regulation is roughly determined by dividing the output impedance of the pass device by the loop gain. To achieve optimal load regulation, the loop gain should be set to a high value since the pass device's output impedance cannot be adjusted.

•**Temperature Drift:** The temperature coefficient characterizes the change in the output voltage caused by the reference's temperature drift and the error amplifier's input offset voltage. Equation 1.4 provides the temperature coefficient.

$$T_C = \frac{1}{V_{out}} . \frac{\partial V_{out}}{\partial T_{emp}} \tag{1.4}$$

$$T_C = (\frac{1}{V_{out}} . \frac{\Delta V_{TC}}{\Delta T_{emp}}). \tag{1.5}$$

$$T_C = (\frac{\Delta VTC_{ref} + \Delta VTC_{vos}}{\Delta V_{out} . \Delta T_{emp}}) . (\frac{V_{out}}{V_{ref}}) \tag{1.6}$$

The dropout voltage of an LDO regulator determines both the maximum current and the minimum voltage that the battery may have. The pass transistor conditions determine the requirements, which include the lowest battery voltage, maximum load current, and dropout voltage. When designing a LDO system, it is usual to figure out the maximum load current and the minimum supply voltage that the system can handle, while guaranteeing that the pass transistor stays in a saturated condition. A relationship is established by Equation 1.7 between the dropout voltage of a LDO regulator and the different specifications related to the device. The maximum

output current flow that the device will tolerate without sacrificing operation is represented by I_{Load} in this formula.

$$V_{dropout} = I_{load}.R_{ON} \tag{1.7}$$

To minimize the R_{DSON} of a pass device, raise the source-gate voltage (VSG) and/or W/L aspect ratio. In practical circuits, the power rails connecting to the integrated circuit are V_{IN} and ground. Therefore, the gate voltage cannot be lower than ground. This implies that VSG has an upper limit V_{IN}. The designer has control over the channel width, but the lowest channel length established by the process technology determines the channel length. The pass device is usually as big as feasible within the width, since the width is determined by the die area limitation. In order to properly lower the R_{DSON}, the main challenge is to be able to bring the gate as near to the ground as possible. The maximum load current that may be tolerated is typically the factor that determines the physical size of the pass device, the dropout voltage, and the powers consumption constraints. The maximum current load specification has to be enhanced in order to be able to deal with the extra parasitic capacitances that arise as a consequence of larger device sizing. This, in turn, causes the total wafer size of the pass device as well as the control circuitry to increase. This is necessary to be able to deal with the parasitic capacitances. There is also a need to increase the ground pin current. Determining the ground pin current and meeting area criteria may be difficult, especially when a very high load current is involved.

1.8.2 Dynamic State Specifications

The dynamic state requirements of an LDO regulator outline its capacity to control the output voltage under load and line transient scenarios. To minimize output voltage fluctuations, the LDO regulator has to react quickly to transients. In contrast to steady state requirements, dynamic-state specifications rely on the large signal LDO regulator characteristics.
Load currents that increase from zero to the utmost value specified cause the most significant fluctuations in output voltage. The load current fluctuation that is shown in Figure 1.12 is the worst case scenario, in which the load current suddenly changes from its highest value to its lowest value and then back again a few times. A model of the fluctuation in the output voltage

may be found in Equation 1.8.

$$\Delta V_{out} = \frac{I_{out}.\Delta t}{C_{out}} \tag{1.8}$$

The regulator's capacity to efficiently handle sudden variations in current load depends on several elements, such as the load current, the output capacitor, as well as the settling time of the LDO regulator.

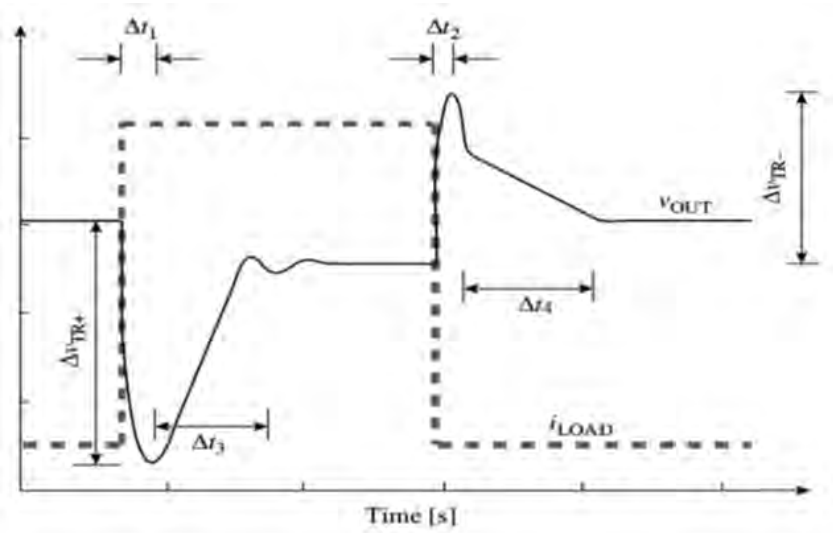

Figure 1.12: Typical transient reaction to sudden load current changes

The reaction time Deltat to these transient glitches is given by Equation (1.9), and it may be expedited by raising the output capacitance C_{out}. A bigger BW_{CL} indicates a larger quiescent current. Output capacitor-less LDOs hence show poor load transients, in contrast to conventional LDOs. How long it takes for the output voltage to settle down during load transients is determined by the open loop phase margin and Deltat. The loop response time t is determined by adding the slew-rate time t_{SR} to the closed-loop bandwidth inverse of the LDO (BW_{CL}).

$$\Delta t \approx \frac{1}{BW_{CL}} + t_{SR} \tag{1.9}$$

$$t_{SR} = \frac{C_P.\Delta V_P}{I_{SR}} \tag{1.10}$$

The primary objective of pass transistors is to achieve a minimal dropout voltage, which contributes to a diminished V_{Dsat} when operating at maximum current. As a result, these transistors generally exhibit increased physical dimensions, which gives rise to a substantial parasitic capacitance (Cp) at their gate. Charge and discharge of the gate capacitance are necessary for the pass transistor to be turned on or off, respectively. The time period of this operation has a direct influence on the pace at which the pass transistor may respond to changes. A slew-rate reduction will result from the extended charging and discharging times required due to an increased gate capacitance. The gain bandwidth product is a metric that represents the maximum frequency at which a circuit may effectively amplify signals. A situation in which the slew-rate exceeds the gain bandwidth product (GBW) indicates that the switching speed of the transistor is relatively rapid when compared to the circuit's amplification capabilities. In this case, the pass transistor responds quickly to rapid variations in load current, allowing for prompt and precise adjustment of the output voltage. To minimizing substantial transient fluctuations at the output voltage node during fast load transients, the reduced reaction time becomes an extremely important factor. Enhancing dynamic performance and ensuring stable voltage regulation in the LDO system requires efficient control of gate capacitance optimization. This is a crucial component. To get the best possible performance, it is essential to make certain that the pass transistor was designed and sized appropriately, as well as the related circuitry, which includes the gate driver and the biasing network.

1.8.3 High Frequency Specifications

Power supply rejection ratio (PSRR) and regulator output noise are considered high frequency parameters [8]. These parameters are regarded to be small signal characteristics and are shown as a function of frequency. Several LDO regulators pinpoint noise at a given frequency that is beyond the gain bandwidth product. These regulators define the PSRR at certain frequencies. PSRR defines the LDO regulator's rejection range for high frequency noise present in the input line. It is related to the loop gain inversely and depends on the parasitic capacitance's of the pass transistor. The error am-

plifier plays a key function in increasing PSRR. The PSRR, expressed as a ratio and formally specified in Equation (1.11), is an essential statistic for evaluating the regulator's performance.

$$PSSR = 20log_{10}.\frac{V_{out,ripple}}{V_{in,ripple}} \tag{1.11}$$

The transconductance of the input stage exerts the most substantial influence on the output noise, whereas subsequent stages make negligible contributions to the overall noise. Improving the size of the input transistors is essential in order to reduce the amount of noise that is produced. Because there is not enough information, it is difficult to do a full study, and the best noise figure changes depending on the particular design being considered. An LDO design that has been simplified is shown in Figure 1.13.

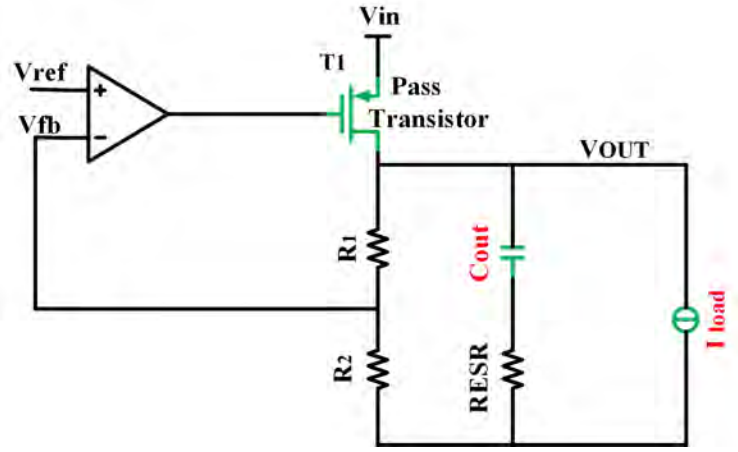

Figure 1.13: A simple LDO architecture

A LDO regulator's efficiency may be calculated by dividing its output power by its input power. The following formula may be used to calculate efficiency:

$$Efficiency = (\frac{Output}{InputPower}) * 100 \tag{1.12}$$

$$Efficiency = \frac{I_{load}.V_{out}}{I_{in}.V_{in}} \tag{1.13}$$

These changes depending on the load, particularly high and low current loads. For light loads, use the following formula:

$$Efficiency = (\frac{I_{load}}{I_{load} + I_Q}).(\frac{V_{out}}{V_{in}}) \tag{1.14}$$

A LDO often has a decreased voltage conversion efficiency, which is shown by the output-to-input ratio. Several factors contribute to this phenomenon, including a low load-input power, the presence of quiescent current, and the impact of dropout voltage. Quiescent current refers to the amount of current that is used by the LDO internally. This means that a part of the input power is used for internal operations instead of being sent to the load. When it comes to dealing with small loads, this becomes an especially troublesome situation since the economic efficiency falls. As a solution to this problem, low power devices (LDOs) that have very low quiescent currents are being created for applications that need little power. This gives them the ability to function more effectively in situations and situations like these.

1.9 Specifications Trade-Offs

The parameters of the LDO regulator are interconnected and result in significant trade-offs. The efficiency, stability, and transient response parameters are the greatest of all the others. The optimization becomes quite complicated, particularly when there are strict constraints. It will be easier to see the trade-offs while developing the LDO regulator.

1.10 Motivation and Objective

The demand for accurate voltage regulation, efficient power management, and optimal performance in various applications such as wearables [10], communication [11], industrial automation [12], automotive, and medical [13] field has rendered LDOs essential components in modern electronic systems. The primary motivation for developing and implementing LDO regulators is to provide accurate voltage control, optimize power management, reduce noise, ensure rapid reaction to abrupt changes, and seamlessly integrate into various electronic systems. As technological advancements demand lower supply voltages in circuit designs, LDOs become the favoured method of supplying numerous voltage levels with a low dropout voltage [9].

1.11 Thesis Organization

The thesis is divided into five chapters. Chapter 1 provides an overview of voltage regulators, including their properties and system level implications. Chapter 2 summarizes current research and provides a quick assessment of prior studies. Chapter 3 describes an LDO voltage regulator circuit with a comparator as a Transient Enhancement circuit and provides simulation results. Chapter 4 depicts another block/schematic level composition of the researched low power LDO voltage regulator with no external capacitor in CADENCE, outlining how each block is created and its performance, as well as the circuit's simulation findings. Finally, Chapter 5 concludes this work.

Chapter 2

State-of-the-Art Research

This thesis focuses on developing an ultra low power, capacitor-less LDO regulators. The examination includes the study, analysis, and implementation of numerous cutting edge methodologies for such circuits. The chapter presents a number of state-of-the-Art research.

High power supply rejection (PSR) throughout a large frequency spectrum is becoming more important in complicated system-on-chip (SOC) designs, notably in LDO regulators. Although traditional LDOs excel at PSR inside their loop bandwidth, their ability to reject supply changes declines when the loop gain falls outside of this range. Furthermore, LDOs with external filtering capacitors often display spectrum peaking in their PSR response, leading in high system level supply noise. This research presents a new technique to designing a LDO regulator that achieves an impressive power supply rejection (PSR) of over 68 dB up to a frequency of 2 MHz. This design can handle various loads of up to 250 mA. To increase the PSR bandwidth, a current mode feed-forward ripple canceller (CFFRC) amplifier is used, offering a maximum of 25 dB improvement in PSR. Crucially, the feed-forward route gain naturally aligns with the LDOs forward gain, obviating the need for calibration [14].

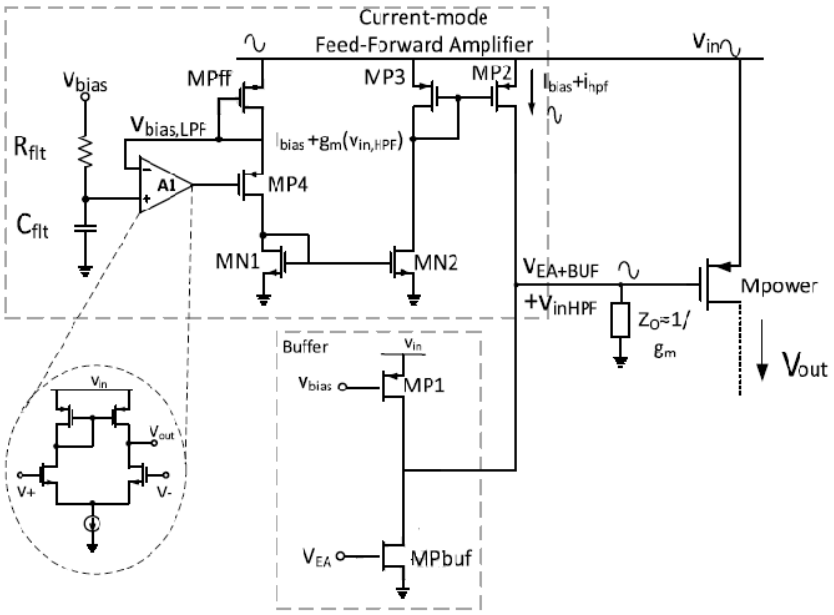

Figure 2.1: CFFRC amplifier with source follower buffer

A capacitor-less LDO that is particularly designed to provide power to high demand mobile applications with heavy loads is introduced. It boasts an exceptional load current capacity of up to 600 mA. The regulator utilizes a unique buffer and feed-forward circuits to provide stable operation, rapid response, and a high unity gain frequency of 2.85MHz at a current of 100mA. This is accomplished by using a total compensation capacitance of 5.1pF. The LDO demonstrates efficient operation throughout a wide input voltage range of 1.5–5.0 V, owing to its low V_{DD} construction. The chip is fabricated using a 0.18μm CMOS technology and has a minimum length of 0.5μm. It has a small size of 0.082mm2. The suggested design has an impressive power supply rejection ratio of -52 dB at a frequency of 100 kHz. The inclusion of buffer and feed forward channels enhances the speed of the system's responsiveness to changes and improves its ability to reject disturbances in the power supply, even when using a smaller compensation capacitance. The buffer facilitates a broad range of output voltage, counteracts the influence of pole induced effects, and sustains a maximum load current of 600mA, making

it highly suitable for mobile applications. The low V_{DD} architecture allows for functioning across a broad range of input voltages. The efficacy of the capacitor less LDO design is confirmed by both experimental and modeling findings [15].

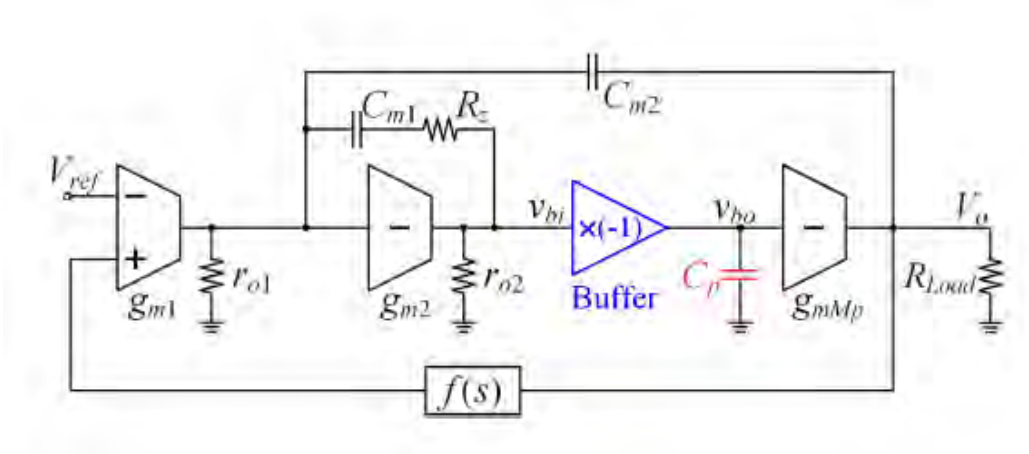

Figure 2.2: Three-stage capacitorless LDO structure with an inverting buffer

A LDO regulator with a rapid settling response is developed. The LDO delivers a consistent 1V output from a 3.0V supply capable of discharging to 1.5V while operating within the range of 0 to 150mA full load current. The PSRR of the LDO is noteworthy due to the utilization of 0.18μm CMOS technology and a folded cascade operational amplifier that includes additional cascade transistors in the error amplifier. When connecting the error amplifier to the pass transistor, a buffer stage is used to improve transient responsiveness. The charging time is further reduced by using a current boost circuit. The settling time is 43.8 ns, and the findings show a little overshoot of 10.51 mV. Starting at 8.895 kHz and going beyond -70 dB all the way up to 136.218 MHz, the PSRR is recorded at -84.464 dB. A value of 174.2μV/V for line regulation and 0.001626 mV/mA for load regulation have been ascertained. To improve the transient response, optimizing the error amplifier means striking a balance between the trade offs of bandwidth and gain [16].

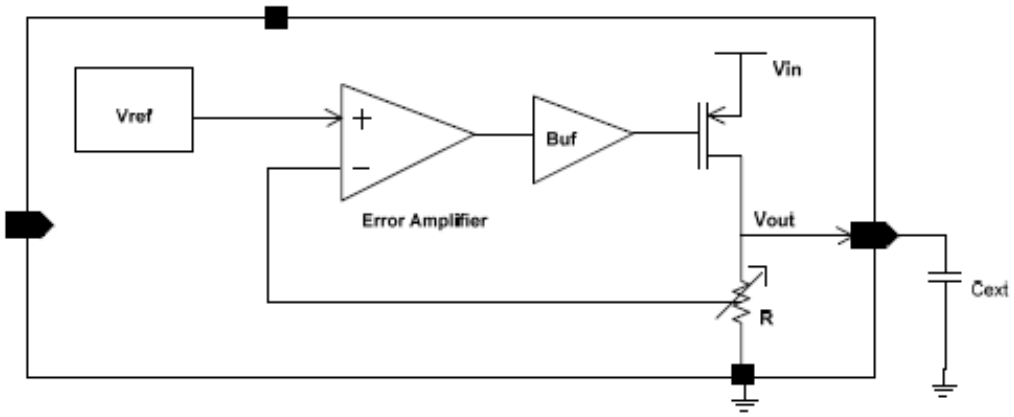

Figure 2.3: Fast Transient Response LDO

The design of a LDO regulator that employs a current feed-back amplifier (CFA) to provide effective supply regulation in deep-submicron analog baseband and RF system-on-chip designs is described. The CFA based LDO exhibits a fast reaction and elevated slew rate while functioning in Class-AB mode in this setup. Significantly, it surpasses a voltage feedback buffer LDO of the same level in terms of settling time, providing a response that is 60 quicker (0.6μs settling time for a 25-mA load step). The suggested LDO occupies a small 0.23mm^2 silicon area and is produced with five metal layers utilizing a 0.25-μm CMOS technology. The PSR at 100 kHz and the output noise spectral density of 67.7nV/Hz are important performance parameters for this LDO. In order to mitigate the effects of lower load capacitance, the CFA buffer included into the design also has a supply ripple reduction step. This characteristic enhances the LDO's overall capacity for a quick transient reaction [17].

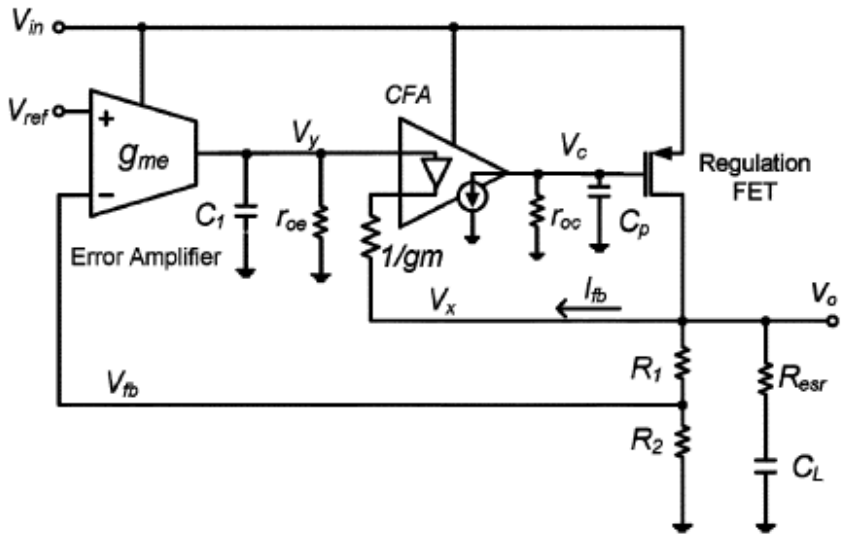

Figure 2.4: LDO architecture using CFA based buffer amplifier

An overview of a LDO regulator design that functions without an output capacitor is discussed which achieves stability through the implementation of feed-forward compensation. LDO stability is maintained across varying load currents and capacitors by means of a flipped-voltage-follower (FVF) configuration in the power stage, which also incorporates feed-forward compensation. The utilization of a minimal 1pF compensation capacitor yields a quiescent current of 28μA when in active mode and 3μA when in low power (LP) mode. The activation of an automatic LP mode switching mechanism by a load current sensor guarantees operation at extremely low power levels. The TSMC-65nm technology implemented LDO operates at a potential of 1.2V and produces an output voltage between 0.9V and 1.1V. The device exhibits an undershoot/overshoot of approximately 250mV for a load current of 10mA and a settling time of less than 1μs. With a bandwidth of 2.1MHz, this dual mode LDO is optimized for loads with currents ranging from 0 to 10mA and capacitances from 0 to 100pF. Situated as a viable option for linear regulator applications at the system level, the proposed LDO is distinguished by its compact silicon footprint, low power consumption, and automatic mode-switching capability [18].

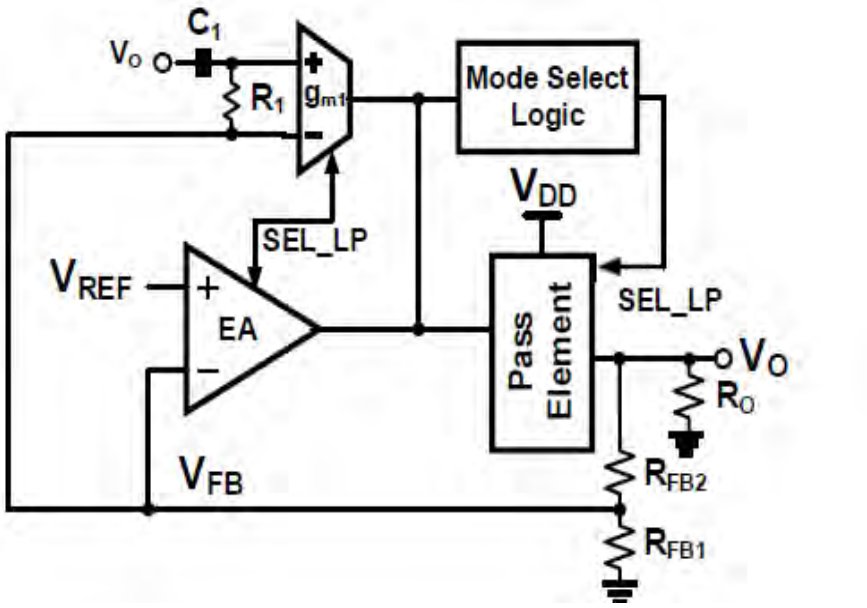

Figure 2.5: LDO with active and low power modes

An innovative method for compensating high current NMOS (LDOs) regulators by using impedance adaptation is developed. The suggested approach aims to enhance the impedance of low-frequency nodes at higher levels, while efficiently decreasing the impedance at high frequencies. This design successfully provides a combination of high gain and a desirable transient response, so reducing the need for a power intensive driver circuit and promoting a simpler and more energy efficient design. In addition, a load tracking methodology is implemented to mitigate fluctuations in load current, thus improving the frequency and transient reactions throughout a wide range of loads. Produced using a 0.35μm CMOS process, the integrated circuit maintains an output voltage configurable between 0.8 V and 1.8 V. It also possesses a 6A current capacity and a maximal dropout voltage of 114 mV. The measurement outcomes indicate overshoot and undershoot voltages of 35.4 mV and -32.2 mV, respectively, during load transitions that occurred between 400 mA and 5A. The load and line regulations at 10 kHz and 1 MHz are recorded as 0.7 mV/A and 0.12 mV/V, correspondingly, with power supply rejections of -55 dB and -30 dB. Increasing the impedance at the gate of the NMOS pass

transistor is one of the ways that the impedance adaption design improves open-loop gain, transient response and energy efficiency. A quiescent current of 0.79 mA is one of the exceptional performance qualities that the LDO has overall. This current is measured under circumstances of zero load [19].

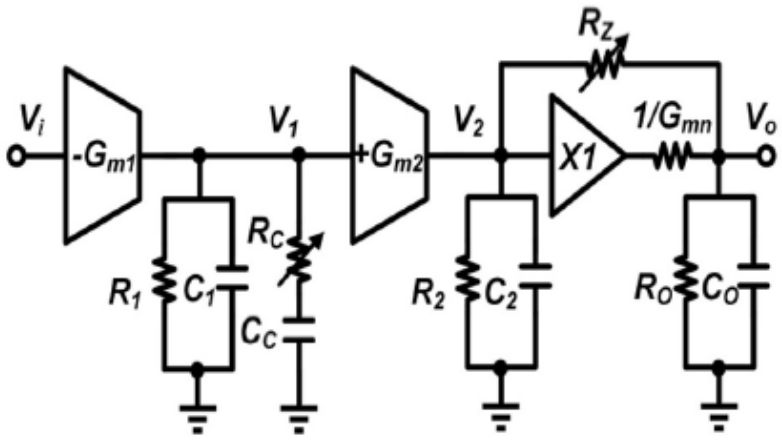

Figure 2.6: Load-tracking and Impedance Adapting Compensated LDO

A LDO regulator that does not need a capacitor and is intended for use on-chip is given. The regulator has a Class-AB input stage with a cross coupled differential amplifier to increase slew rate, as well as a passive low-pass RC filter for improved PSRR. The operational transconductance amplifier (OTA) in the Class-AB input stage enables a high DC gain, resulting in a power supply rejection ratio (PSRR) of about 45 dB at a frequency of 100 kHz. In order to improve the power supply rejection ratio PSRR, the LDO design includes a pMOS pass transistor connected in series with an nMOS device. The implementation of Miller capacitance assists in stabilizing the LDO when it is connected to a modest 10pF load capacitor. The first simulation findings suggest that the proposed LDO regulator may operate well with a supply voltage range of 3.3-3.5 V. The test results indicate that the dropout voltage is at least 0.5 V when the load is at most 50 mA, and the quiescent current is 50μA [20].

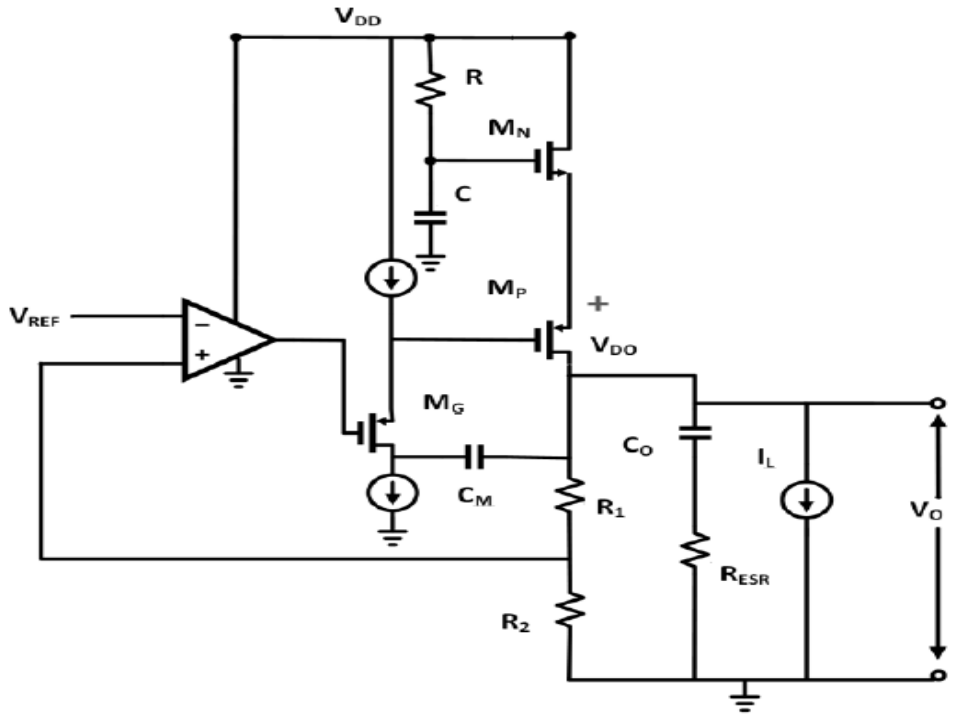

Figure 2.7: Capacitor-less LDO with improved PSRR and enhanced SR

The development of a capacitor-less LDO regulator with the goal of enhancing PSR and Figure-of-Merit (FOM) in switching devices, particularly for display driver ICs is described. The proposed LDO regulator incorporates advanced circuitry to effectively reduce power supply noise across a wide frequency range, resulting in improved performance. The regulator is produced utilizing a 0.18μm CMOS technology and demonstrates exceptional performance. It achieves a power supply rejection ratio (PSR) of -76 dB at 1 MHz and a Figure-of-Merit (FOM) of 96.3 fs. Remarkably, the regulator maintains these parameters even when the overall on-chip capacitance is as low as 12.7pF. The capacitor-less LDO regulator is designed to meet the needs of completely integrated switching devices that need strong PSR and outstanding FOM in a small size [21].

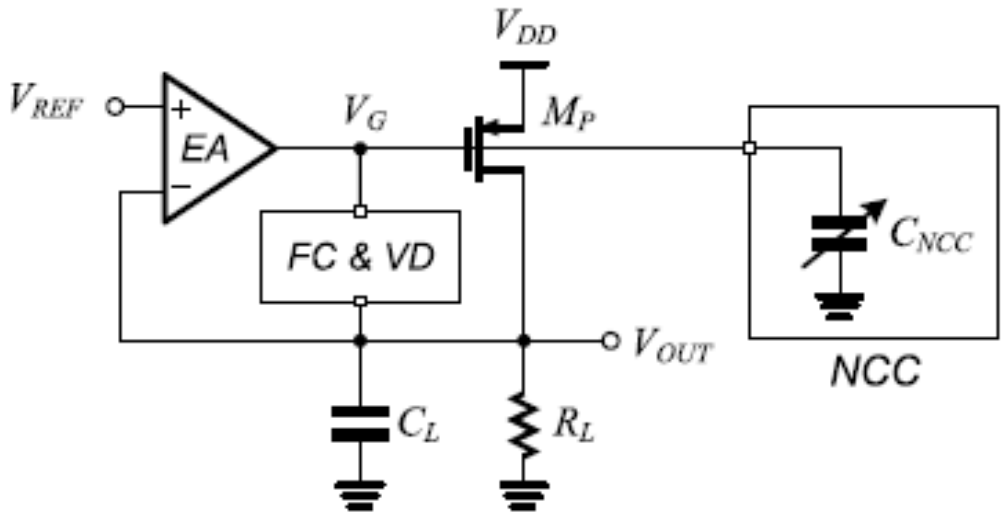

Figure 2.8: Fundamental blocks of the proposed LDO regulator

A novel frequency compensation and slew-rate booster circuit designed especially for automotive applications using LDO regulators is developed. Three major issues with LDO design are successfully handled by the circuit: it can handle a wide variety of output currents and load capacitors; it guarantees a quick reaction to load transients; and it reduces susceptibility to supply changes. The LDO configuration that was suggested has been incorporated into the proposed circuit; it is capable of delivering a 5V output voltage as well accommodating a maximum 50mA output current over a broad temperature and supply voltage range of 5.25V to 40V and -40 °C to +150 °C; it consumes a small 30μA. In order to prevent output voltage overshoot and undershoot caused by abrupt load changes, the slew rate booster is of critical importance. In addition, the LDO satisfies the E-06 test criteria specified in the LV124 automotive standard, guaranteeing output voltage stability even in the event that sinusoidal voltages are introduced into the supply line. Interestingly, the circuit uses a minimum 1μF output capacitor to obtain these results, which is far lower than similar LDOs. The design has been validated through extensive simulation and measurement processes; it is based on a CMOS Op-Amp slew-rate booster and has proven to be stable and perform exceptionally well in demanding automotive environments [22].

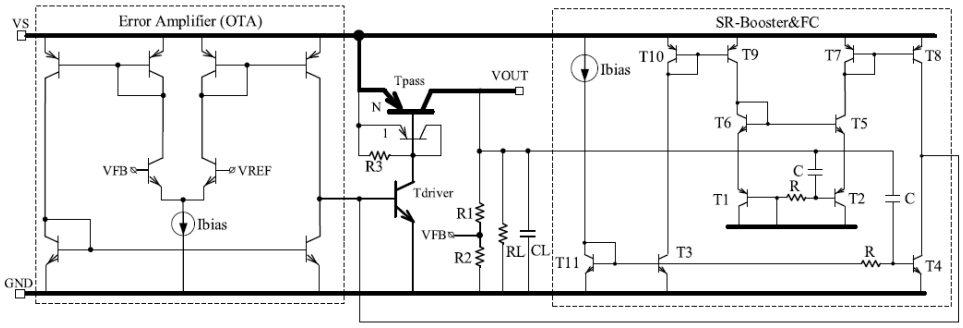

Figure 2.9: LDO based on the enhanced SR-Booster and FC introduced

Chapter 3

LDO with Comparator

This chapter examines a complete method to constructing a CMOS analog circuit supplying fully integrated LDO. The LDO regulator used in this study is designed on the CADENCE Virtuoso platform in 55nm bulk CMOS technology.

3.1 LDO Architecture

The first capacitor-less LDO regulator especially designed for system-on-a-chip (SoC) applications. Ensuring the circuit's stability across all loaded currents is of utmost importance, particularly when handling low load currents. Moreover, it is imperative that the circuit exhibits suitable responses to abrupt fluctuations in load. The goal of the design guidelines is to use a low voltage topology to ensure satisfactory regulation performance while minimizing power and area consumption. The specifications are customized to meet our specific requirements, with the objective of achieving a 0.8 V output voltage V_{out} that is compatible with a 1V supply voltage V_{in}, while operating within a temperature range of -40 to 120 degrees Celsius. In addition, a settling time of 0.2μs and a maximal load current I_{Load} of 50 mA must be maintained by the design.
This study presents a LDO regulator that does not rely on an external capacitor and has an extraordinarily rapid transient response. The LDO regulator employs comparators in conjunction with a low power operational transconductance amplifier to control the gate of the pMOS pass element. The comparators enable the regulator to promptly react to transients in the load or

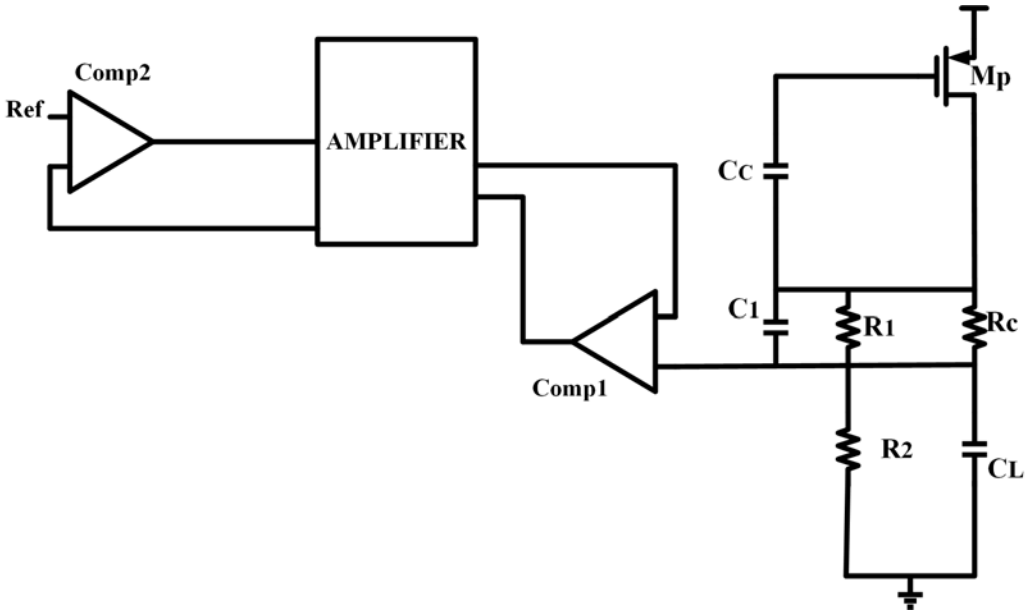

Figure 3.1: Block diagram of the LDO regulator

line.

3.2 Circuit Realization and Schematic

The following section will present a comprehensive review of the schematic's fundamental components and the execution of the enhancement framework. Figure 3.2 illustrates the schematic representation of the external capacitorless LDO that has been proposed [23]. Setting the voltage at the gate of the pMOS pass element to a value that corresponds with the current passing through the load is accomplished using a single stage operational transconductance amplifier (OTA).The M2 switch is used to counteract V_{OUT} undershoot, whereas the M7 switch is employed to mitigate V_{OUT} overshoot. When the comparator Comp1 detect an undershoot, it activates switch M2, causing the V_{GAT} to move towards ground and increasing the supplied current. The OTA's speed increases when M2 is activated because to the reception of an even stronger bias current. Therefore, Comp1 also functions like a dynamic biasing circuit. To correct the overshoots, switch M7 is activated by com-

parator Comp2. This causes V_{GAT} to be drawn toward V_{DD}, thereby reducing the current and preventing an increase in the output voltage. The offsets of the two comparators are calibrated so that, under constant conditions, they remain deactivated and solely become active when there is an overshoot or undershoot.

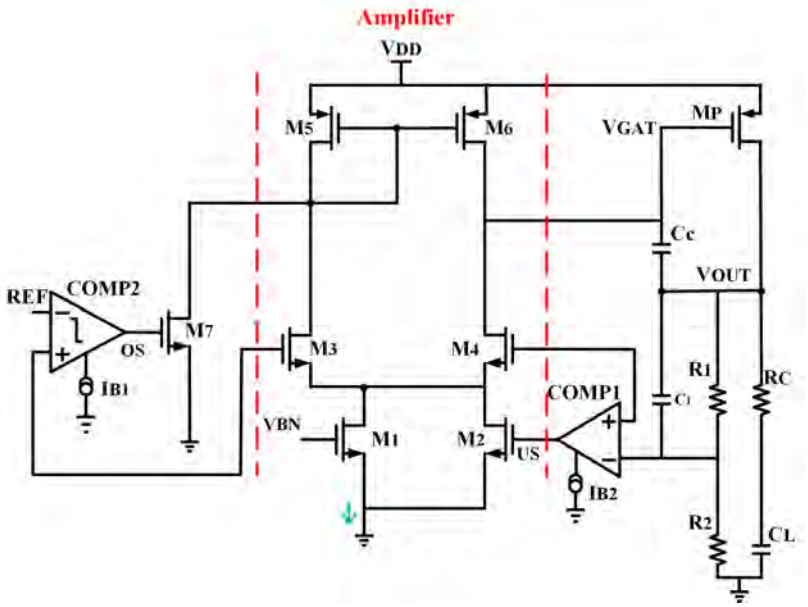

Figure 3.2: Schematic diagram of the CL-LDO circuit

Presented in Figure 3.3 is the schematic representation of the comparator that has been developed. This device makes use of a conventional differential stage that is equipped with cross coupled transistors. To increase the amount of current that is pumped into the comparator during the regeneration phase, an extra positive feedback loop that is made up of transistors M7, M9, and M8 is added. This ultimately results in a faster process. This current will only be present when the comparator is in the "on" position, which is only possible when an undershoot or overshoot is compensated for. The inclusion of capacitance Cc in Figure 3.2 serves the passive purpose of assisting in the compensation process for the output voltage variation. In order to offset the alteration in V_{OUT}, Cc influences the modification in V_{GAT} in the same manner as the change in V_{OUT}. The presence of a capacitor serves to

mitigate the extra delay caused by the resistive voltage divider and the input capacitance of the (OTA) by redirecting the alteration in the output voltage back to the OTA input and the comparators. The resistor Rc serves as a sensing resistor for quantifying the fluctuations in the output voltage. The function of the amplifier is to increase the fluctuations in the output voltage resulting from the voltage decrease across the capacitor, which happens when current passes from the capacitor to the load. This enables the comparators to identify the change at the beginning of line or load transient. In steady state, the resistor is not subject to any losses since there is no current passing through it after the output voltage has reached a stable level.

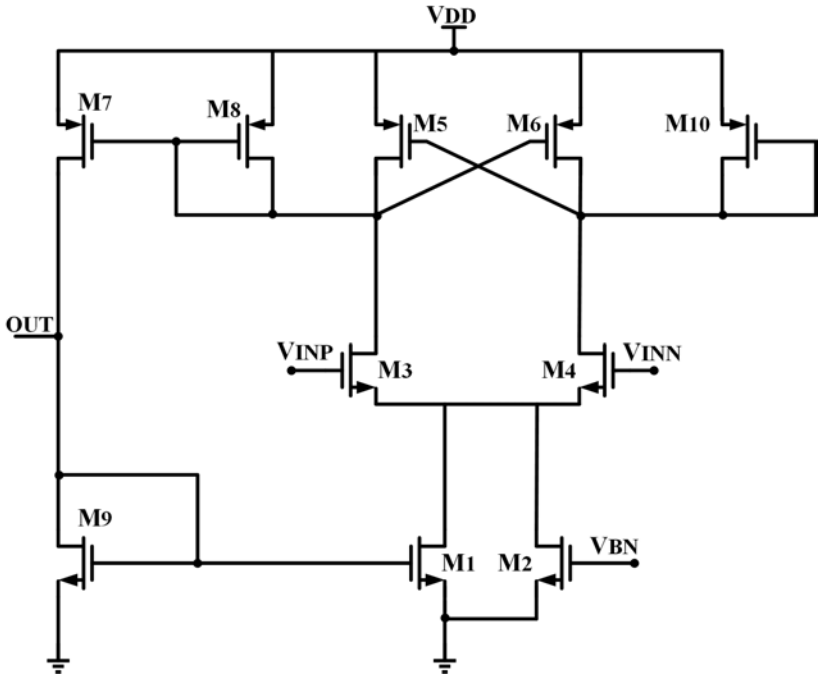

Figure 3.3: Circuit diagram of comparator

3.3 Reducing Overshoot and Undershoot

The primary characteristics of LDO are undershoot and overshoot. Optimizing the undershoot and overshoot of the circuit improves its overall performance. Throughout the design process, the LDO designer used several techniques to mitigate the occurrence of overshoot and undershoot in the circuit. A decrease in the output voltage can be observed when there is a sudden surge in the load current, leading to the discharge of the small on chip load capacitor. A potential factor contributing to an undershoot is an abrupt reduction in the supply voltage, which may be caused by a substantial voltage drop within the supply's internal impedance, for example. Overshoots occur when the supply voltage or load current abruptly increases or decreases. In response to an undershoot detected by comparator Comp1, switch M2 is activated to increase the supplied current by pulling V_{GAT} towards ground. When M2 is activated, the OTA receives an increase in bias current, which accelerates it; thus, Comp1 also functions as a dynamic biasing circuit. Comparator Comp2 mitigates overshoots by activating switch M7, which drives V_{GAT} towards V_{DD}, therefore reducing the current and avoiding an increase in the output voltage. The offsets of each of the comparators are adjusted in a manner that ensures they remain inactive during the stable condition, and only activate when there is an excessive increase or decrease in the signal.

3.4 Design Specifications

The design specification for the suggested design is shown in Table 3.1. The input voltage is 1V, and the maximum current that may be drawn from it is 50mA. A 1pF capacitor is utilized at the output of the design. The LDO design under consideration achieves a dropout voltage of 200mV, which is the lowest possible.

Table 3.1: Design Specifications

Parameter	Specifications
Input/Output Vlotage	1V/0.8
Line Regulation	0.068 (mV/V)
Load Regulation	0.004 (mV/mA)
Load Current	50mA (max)
C_{out}	1pF (on-chip)
V_{out}	0.8 V

3.5 Simulation Environment

The LDO regulator in this research has been developed using the 55nm bulk CMOS technology on the CADENCE Virtuoso platform. Table 3.2 and 3.3 presents a thorough overview of the design parameters, which include the (W/L) ratios of all MOSFETs and the values of the capacitors shown in Figure 3.2.

Table 3.2: Aspect Ratios of the Transistors of LDO Architecture

Parameter	W(μm)	L(μm)
M1, M2	6	1
M3, M4	4	1
M5, M6	5	1
M7	2	1
M_{Pass}	2m	1

Table 3.3: Aspect Ratios of the Transistors of LDO Comparator

Parameter	W(nm)	L(nm)
M1, M2	120	60
M3, M4	120	60
M5, M6	240	60
M7	480	60
M8	240	60
M9	480	60
M10	240	60

3.6 Result and Discussion

The output voltage of the LDO regulator with C_L= 0 pF is shown in Figure 3.4. The load transient behaviour of the capacitor-less LDO voltage regulator, which is shown in Figure 3.5, was simulated by employing a load current variation ranging from 0 A to a maximum load current of 1 mA, while allowing for a settling period of 0.2μs. It was determined that the ideal input voltage should be adjusted to the nominal value, which is Vdd = 1V, and the load capacitance should be equal to 1pF.

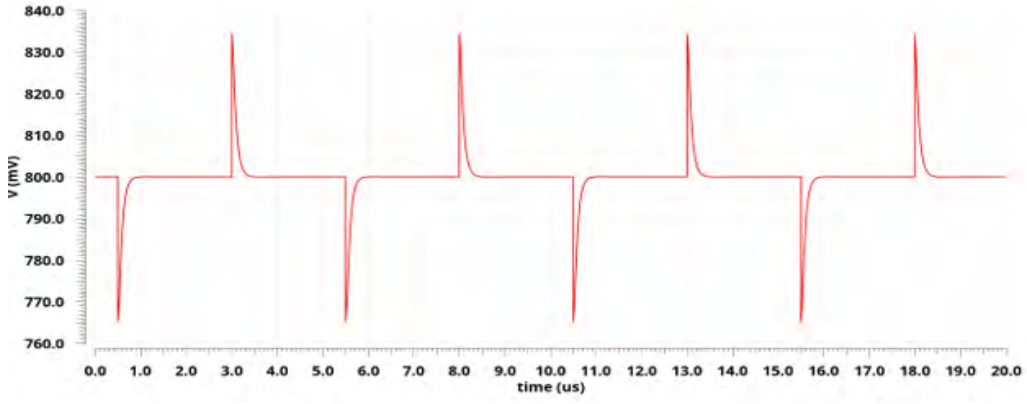

Figure 3.4: Output Voltage of the LDO Regulator with C_L= 0 pF

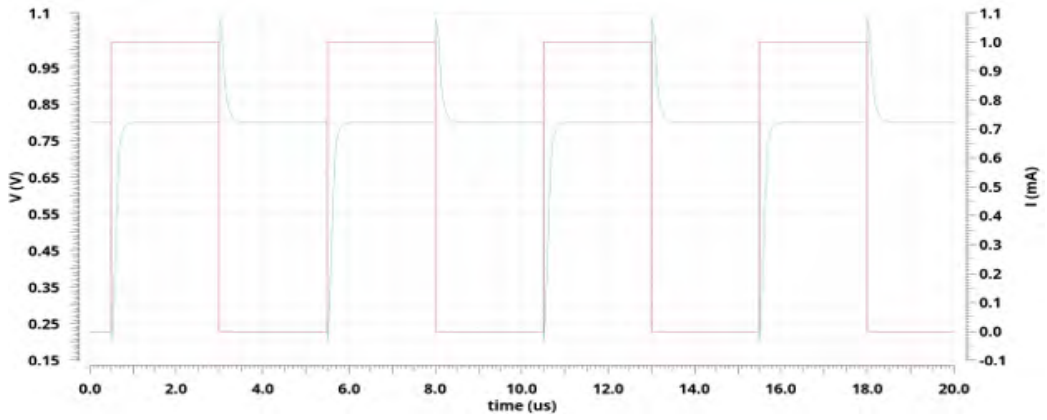

Figure 3.5: Transient simulations for I_L=1mA with C_L=0 pF

The term "line regulation" describes the proportionate change in the output voltage that occurs in response to a particular change in the voltage of the battery. In order to evaluate the line regulation of LDOs, a direct current (DC) analysis is carried out to investigate the fluctuations in output voltage that are brought about by changes in the voltage of the input supply. A representation of the related result may be seen in Figure 3.6. The line regulation is measured to be 0.068 millivolts per volt (mV/V). This indicates that every change in voltage at the input leads to a proportional change in the output, with a magnitude of just 68 millivolts. Figure 3.7 demonstrates the variation of the output voltage in response to fluctuations in the line voltage under typical conditions.

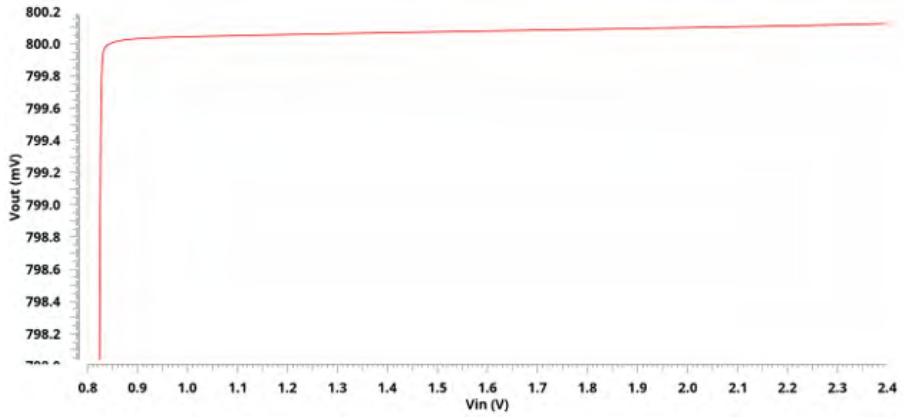

Figure 3.6: Simulated line-transient response with a 0pF off-chip capacitor

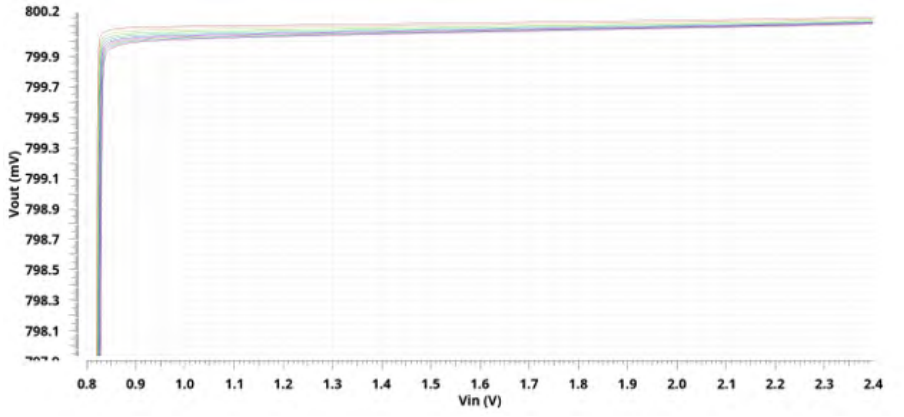

Figure 3.7: Transient simulation results for Temperature change from - 40° to 120°and I_L=1mA with C_L=0 pF

An analysis of the design's performance takes place at various temperatures, as seen in Figure 3.7. The battery voltage is varied in a range from 0.8V to 2.4V. The measured temperature range is from -40°C to 120°C, with 0.02V being the highest recorded value. It has little variation from the target voltage level at low temperatures.
Figure 3.8 illustrates the load regulation response of the regulator, showing the variation in load current from 0mA to 50mA. The data was acquired by

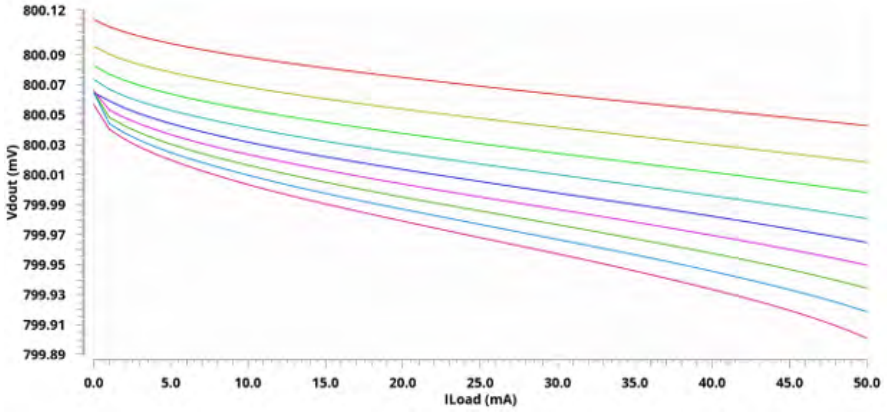

Figure 3.8: The Simulation Outcomes of Load Regulation for V_{in}=1V and C_L=0 F at the temperature variation from -40° to 120°C

CADENCE simulation. The maximum deviation of the output voltage from the expected value is 34mV under normal conditions.

The LDO regulator has a maximum current consumption of 26μA when operating at full load. The total current drawn by the LDO regulator is dependent upon the loading current, as shown in Figure 3.8. The LDO has a minimum input requirement of 1V and a maximum output capability of 0.8V. The power consumption of this circuit amounts to 90μW.

3.7 Layout Design

Figure 3.9 depicts the architecture of the entire LDO voltage regulator. The overall chip area utilization is around (70.02μm $\times$ 24.41μm) . The pMOS pass element and the C_1 capacitor need the majority of the available space, as illustrated.

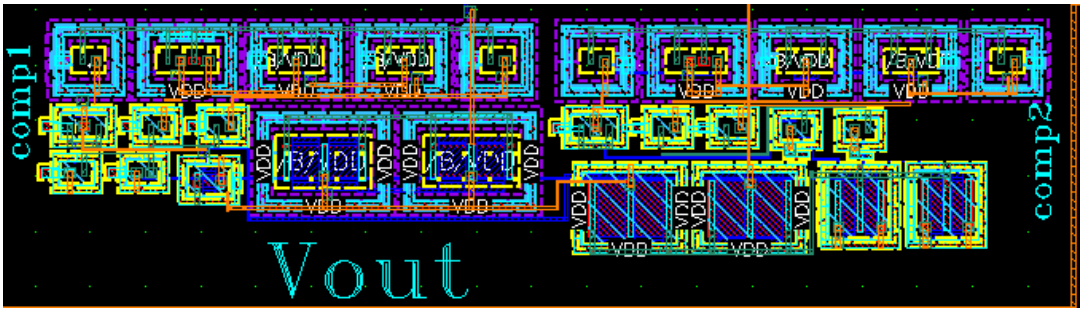

Figure 3.9: Layout of OTA and comparator

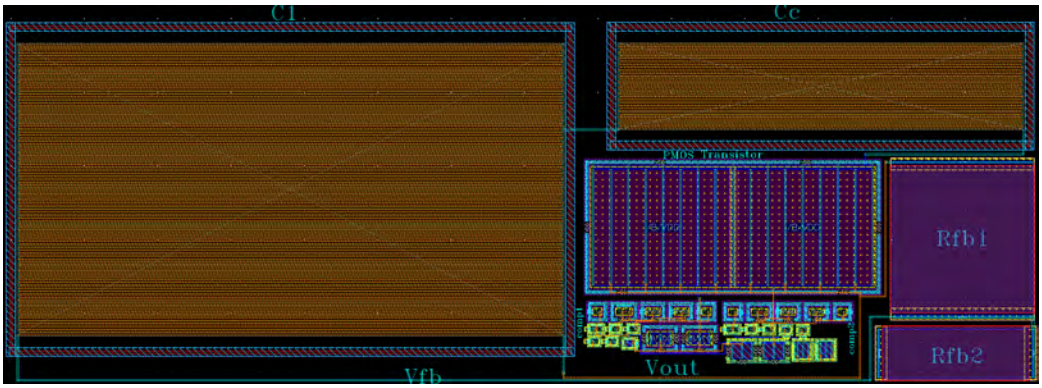

Figure 3.10: Layout of LDO

Chapter 4

LDO with Folded Cascode Amplifier

The LDO regulator's design method is thoroughly explained in this chapter. Every segment of the chapter presents an elaborate description of the design procedure performed for a specific block, that includes the design considerations and the primary factors that were taken into account. The error amplifier, pass transistor, and feedback network comprise the LDO regulator's fundamental construction blocks. The purpose of this chapter is to describe, characterize, and optimize each block before examining how they interact within the LDO regulator.

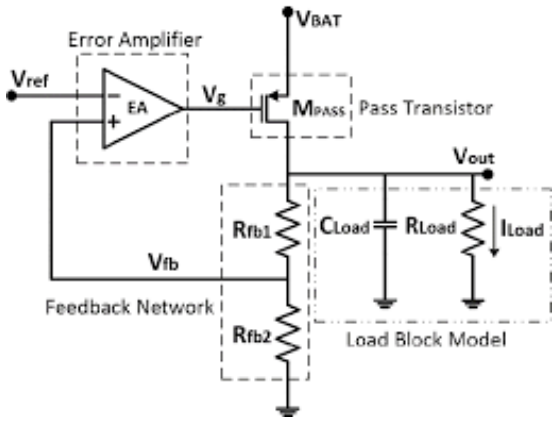

Figure 4.1: Block diagram of Folded Cascode based CL-LDO circuit

4.1 Schematic Architecture

LDO voltage regulators are specifically engineered to work in low-power applications without using an additional capacitor for compensating. Figure 4.2 depicts the complete design of the voltage regulator [24]. So as to make the compensation procedure as easy as possible, the design encompasses just two steps.The system's two stages each add to its total gain and are affected by variations in the power source. Careful consideration is necessary when biasing the devices during both stages.

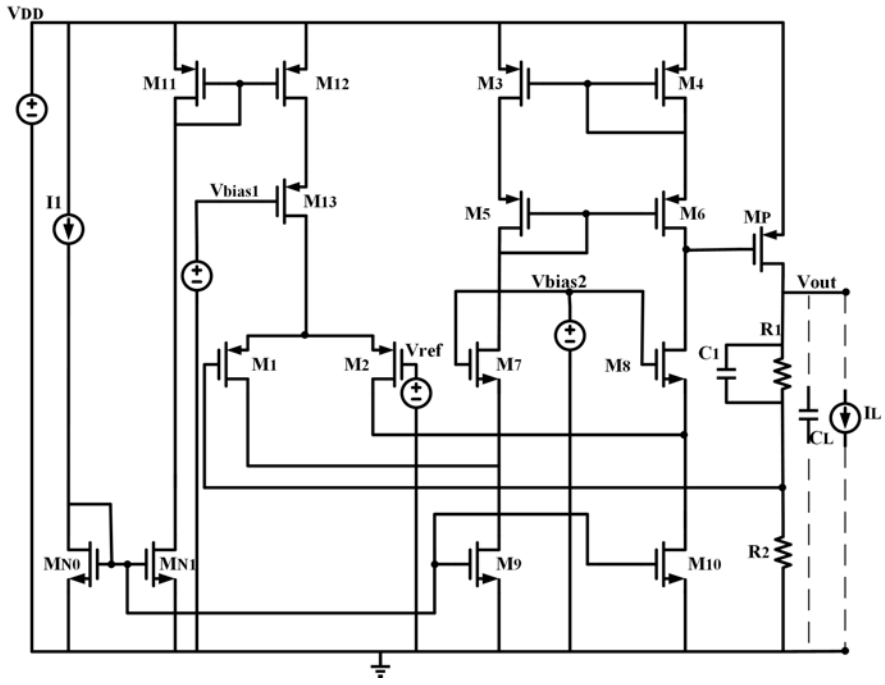

Figure 4.2: Schematic diagram of Folded Cascode based CL-LDO circuit

4.2 Folded Cascode

This is because the first stage is a folded cascode, which allows for a significant amount of gain to be achieved in a single stage. The limited headroom brought on by a low supply voltage led to the folded cascode architecture being chosen over the telescopic cascode. Furthermore, the output swing of a folded cascode is larger than that of a telescoping cascode. Transistors M12 and M13 comprise the cascoded tail current source, while input transistors M1 and M2 are pMOS devices. nMOS transistors M7 and M8 implement the "folded back" common gate of the cascode. M9 and M10 are responsible for supplying this bias current to M7 and M8, respectively. An enhanced Wilson current mirror, comprising transistors M3, M4, M5, and M6, is employed to load the folded cascode. To eliminate the systematic gain error commonly observed in Wilson mirrors, an additional transistor is incorporated into the input side (M3 and M5) in order to equalize the drain source voltages of both transistors that are in closest proximity to the power supply (M3 and M4). The output resistance of the first stage increases when an enhanced Wilson mirror is employed to load it, as opposed to a basic two-transistor mirror. This results in an even greater advantage.

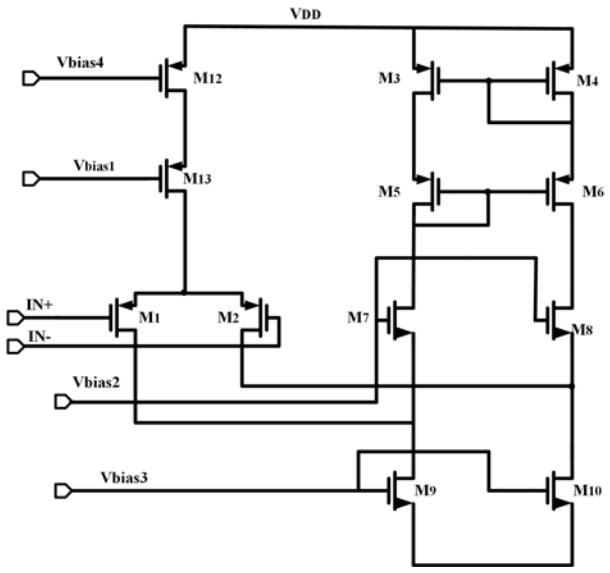

Figure 4.3: Schematic diagram of folded cascode

4.3 Pass Transistor

The PMOS pass transistor MP serves as the LDO's second stage. This device must be quite wide in order to source huge load currents while maintaining a tolerable gate-source voltage. To keep the cutoff voltage as low as possible, the length is kept at its shortest number. At the bottom of MP is where the LDO's output power is. A voltage divider made up of resistors R1 and R2 sends some of the output voltage back to input. The huge sizes of R1 and R2 are selected to allow for very little current to flow through them, lowering the feedback circuit's power consumption.

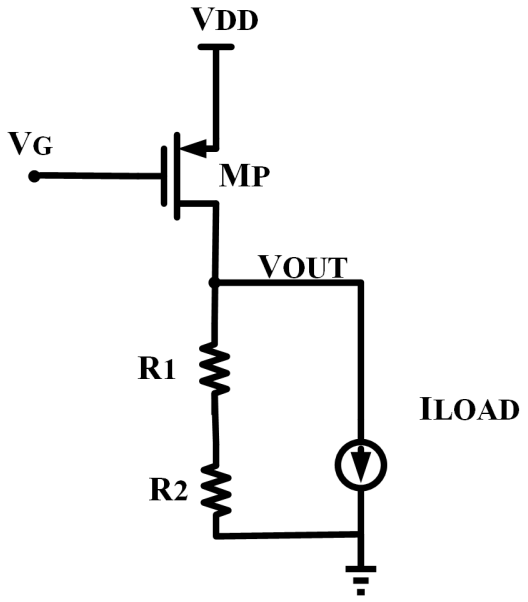

Figure 4.4: Pass Transistor

4.4 System Gain

The first stage's output is directly connected to the second stage's input, which is the MP gate. Because the gate-to-source resistance of a MOS device is so high, interstage loading is irrelevant when attempting to determine the LDO's gain. Adding together the gains from each step yields AC open loop gain. After determining the output resistance and transconductance (gm of M2), the first stage's gain may be determined. The output resistance is made up of the drain impedances of M6 and M10, which are combined in parallel. Multiplying the MP's transconductance by the LDO's output resistance yields the second stage's gain. This is the pair that gazes downward at R1 and R2 from above the MP's drain. The very high DC current in MP causes the r_o to be much lower than the resistance of the series circuit consisting of R1 and R2. Therefore, R1 and R2 may be disregarded when creating the second stage gain statement. Thus, $g_{m2}\ [2g_{m5}\ r_{o3}\ r_{o6}] \parallel [g_{m8}\ r_{o8}\ (r_{o10} \parallel r_{o2})]\ g_{mp}\ r_{op}$ represents approximately the gain of both stages combined. The transconductances of M2, M5, M8, and MP are denoted by g_{m2}, g_{m5}, g_{mp}, and r_{o3}, r_{o6}, r_{o8}, r_{o10}, r_{o2}, and r_{op}, respectively, are the output resistances of M3, M6, M8, M10, M2, and MP. Because the output resistance of MP is minimal in comparison to the output resistance of the other devices, the gain expression clearly shows that the majority of the gain comes from the first stage, as expected.

Table 4.1: Aspect Ratios of the Transistors

Parameter	W(μm)	L(μm)
M_{N0}	5	1
M_{N1}	5	1
M1, M2	15	1
M3, M4	12	1
M5, M6	6	1
M7, M8	4	1
M9, M10	15	1
M11	5	1
M12	10	1
M13	5	1
MP	2m	1

4.5 Biasing

There are limitations that need to be thought about while biasing the LDO's devices. M9 receives current from M1 and M7, as shown in Figure 4.2, whereas M10 receives current from M2 and M8. One half of the current passing through M12 goes to M1 and the other half goes to M2. Bias currents in M9 and M10 must be over half of the bias current in M12 for M7 and M8 to not have a zero bias. An nMOS mirror, the input of which is directly regulated by the ideal current source I1, regulates the bias currents in holes M9 and M10. A pMOS mirror, that provides M12's bias current, takes an extra output from this mirror.

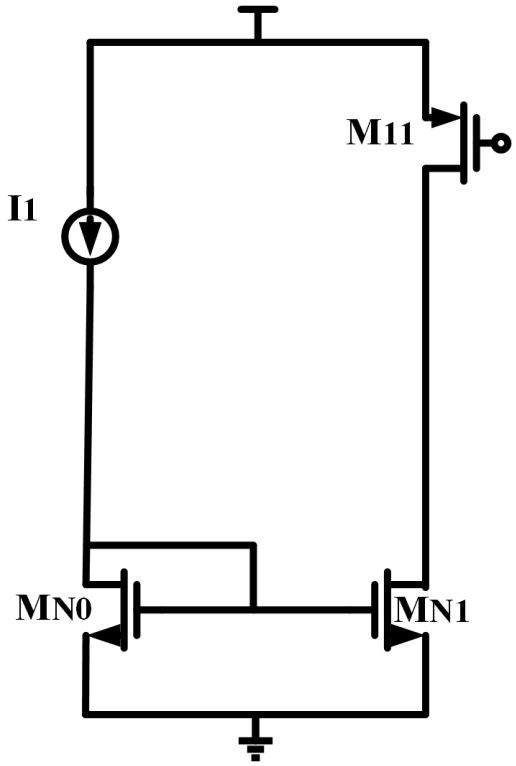

Figure 4.5: Biasing Circuit

To keep the improved Wilson mirror's transistors M4 and M6 in saturation, the combined gate-source voltage of these transistors plus an extra overdrive

voltage shouldn't be higher than the gate to source voltage required by MP. When calculating the necessary voltage, the amount of current that the MP must deliver is based on the load current that the LDO specifies. Due to the current flowing via R1 and R2, MP is required to source a little bit more current than the load current. The feedback network current, however, has been reduced by the load current. It is critical to fine-tune M8's bias current as it shares its current with M4 and M6. Due to the fact that the source-drain voltage of M6 is dictated by the variation (in terms of magnitude) between the gate-source voltage of MPass(MP) and the gate source (and thus drain source) voltage of M4, the saturation limit for M6 is exceeded if the size of M4 is too large. It follows that M10's bias current ought to be robust enough to provide M8 with adequate bias current, but not so excessive that M6 loses saturation.It is also important to set the bias voltages correctly for the transistors M7, M8, and M13 gates. If the voltage at the gates of M7 and M8 is too low, M9 and M10 will be driven out of saturation because their drain-source voltage, which is, in fact, the difference among the gate voltage at M7 and M8 and the gate source voltage needed by M7 and M8's bias current, is equal to zero. Because the voltage at the sources of M7 and M8 is quite near to the voltage at the gate of MP, if the gate voltage is excessively high, they will be forced out of saturation. To keep M13 in saturation, it is necessary to control the gate voltage of M13 so that its source voltage supplies a drain-source voltage that is equal to or greater than that of M12.

4.6 Simulation and Result Analysis

In this section, we will present a study of the transient, DC, and AC parameters of the design that has been discussed.

4.6.1 DC Analysis

DC analysis is a metric that evaluates many aspects of a LDO regulator, such as its operating region and line regulation. The circuit's implementation results in undershoot and overshoot values that are both below 0.1V, and it achieves a settling time of 0.1μs shown in Figure 4.6. The purpose of line and load transient simulations is to assess the transient performance of the implemented LDOs. We apply a line transient step with a rise and fall time of 10 ns from 0.8V to 2V at the input node VDD. The test was carried

out using a continuous load current (I_L) of 1 mA. Figure 4.7 illustrates how the output node V_{OUT} responds to the line transient.

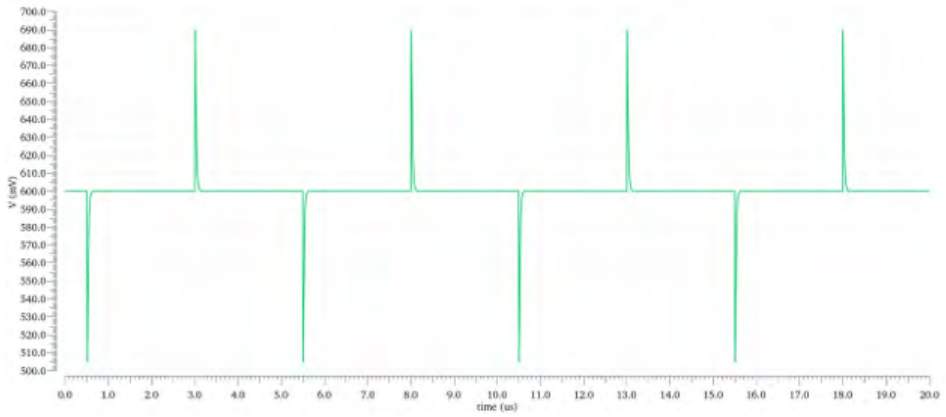

Figure 4.6: Measured Output Voltage of the LDO Regulator with C_L=0 pF

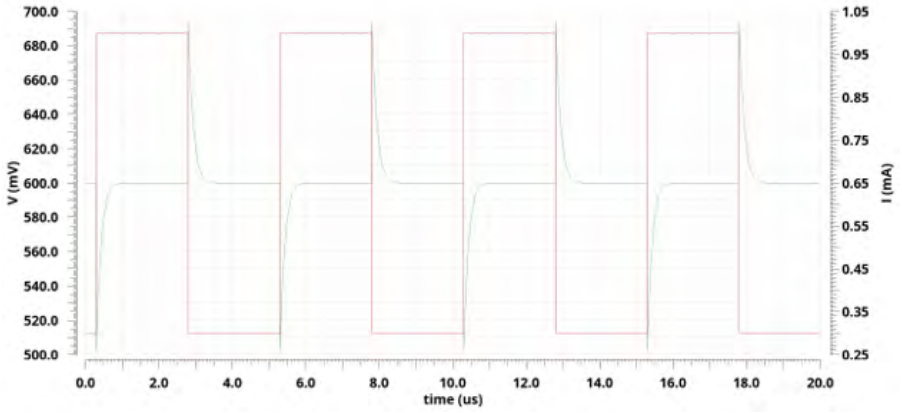

Figure 4.7: LDO transient simulation for Iout from 50mA to 10mA

4.7 AC and Stability Analysis

The gain of the error amplifier is 73.33 dB, and the phase margin is 78 degrees, which gives a very good GBW product of 20.47 MHz. Because Vout is fed to the error amplifier via a resistive feedback network, the overall gain of the system is close to half. It indicates the overall system is stable at maximum load. The frequency response of the circuit is shown in Figure 4.8.

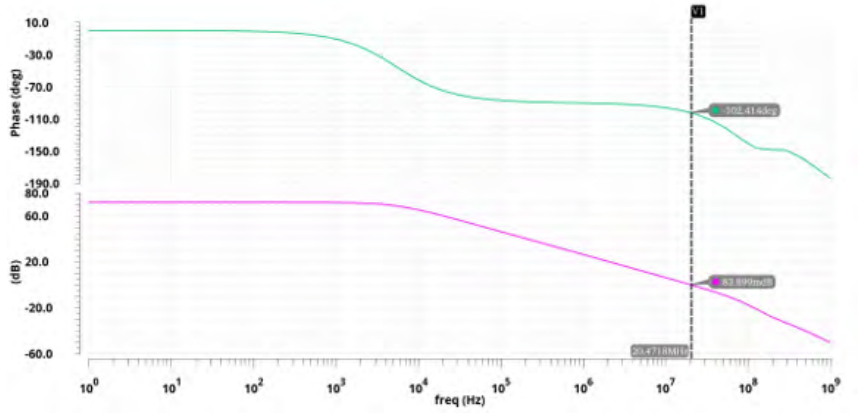

Figure 4.8: Frequency response of the single stage error amplifier

4.8 Line Regulation

Line regulation is a measurement performed on LDO regulator to assess its capacity to maintain a consistent output voltage in the presence of fluctuations in the input voltage. The related outcome is depicted in Figure 4.9. Line regulation is calculated to be 0.045(mV/V).The loop gain has a direct relation to line regulation. The folded cascode design is a good choice because it keeps the phase margin high.

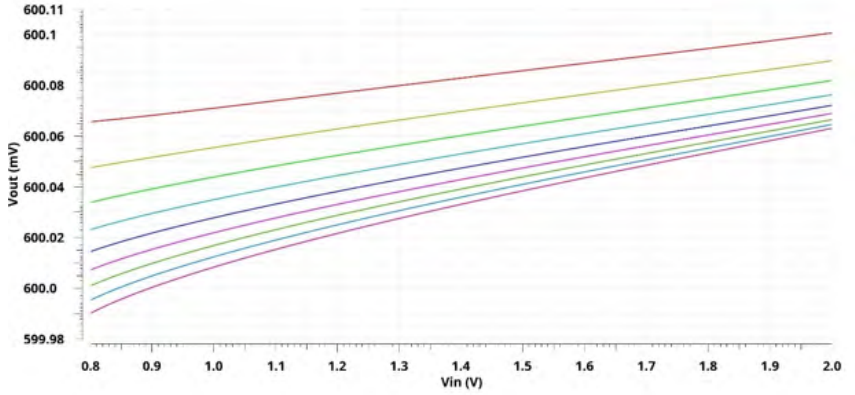

Figure 4.9: The results of the simulation for line regulation with I_L=1 mA and C_L=0

4.9 Achieved Results

Load transient the output voltage's typical response, with rise and fall times of 1ns each, to a change in the current load from 0.1 mA to 50 mA is shown in Figure 4.10. Load regulation measures the capacity of the LDO to uphold a consistent output voltage in the face of fluctuations in the load current. The data was acquired by simulation using CADENCE. Under conditions of dynamic load, it guarantees stability. Under normal circumstances, the output voltage's largest measured deviation from its predicted value is 90 millivolts.Table 4.2 provides a list of regulator design outcomes.

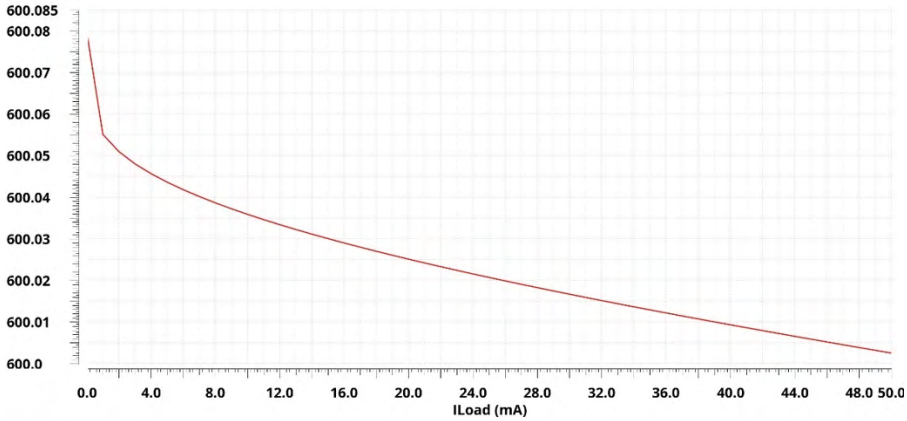

Figure 4.10: Simulated load-transient with for 0pF output capacitor for I_{load}=0 to 50mA

Table 4.2: Summary of Measured Results

Parameters	Specifications	Measurement	Units
Input Voltage	0.8-2	0.8-2	V
Output Voltage	0.6 V	0.6	V
Line Regulation	1	0.045	(mV/V)
Load Regulation	2	0.0014	(mV/mA)
Max.Load Current	50	50	mA

4.10 Layout Design

Cadence Virtuoso is used to implement the proposed design's layout. The design's entire active area is 34.4μm $\times$ 38.7μm. Figure 4.11 and 4.12 depicts the arrangement with all of the capacitors and transistors. For all cell level layouts, Metal 1, Metal 2, Metal 3, and GT are used. Metals 1 and 2 are utilized for capacitors.

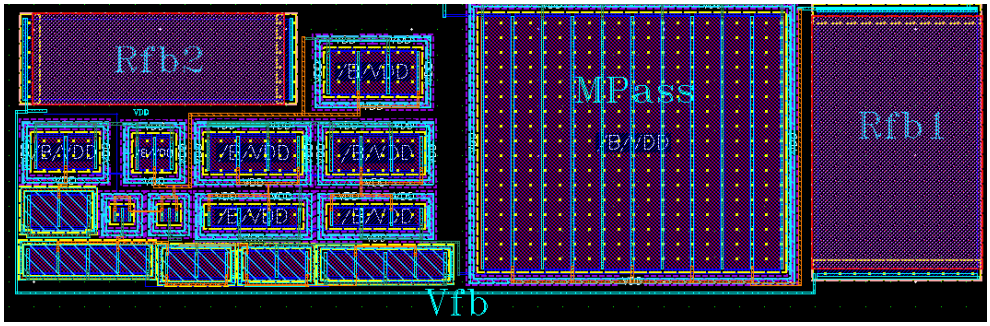

Figure 4.11: Layout of LDO

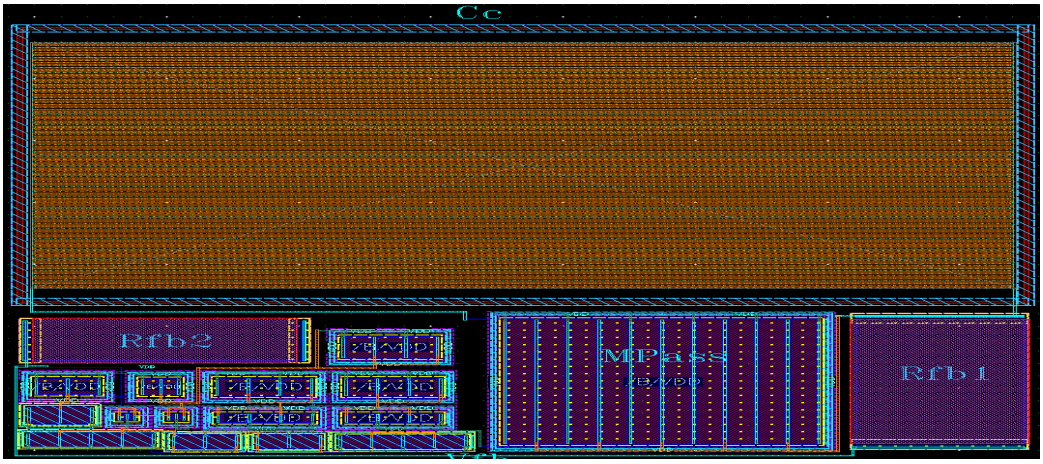

Figure 4.12: Layout of LDO with C_L

4.11 State-of-the-Art Comparison

The measured performance improvement is presented in Table 4.3, which presents a comparison of the efficiency of the LDO that was implemented with a number of different capacitor-less LDO designs that were existing in the past. Because the proposed LDO design works well as a heavy-load regulator, it can be used in a variety of battery-powered systems. The LDOs studied demonstrate a DC load regulation of 0.014 mV/mA, which is done while maintaining a good DC loop gain. This load capability is considered reasonable in comparison to the other LDOs. Achieving effective load control with a large load current is difficult since the loop gain of the LDO reduces with increasing load current in the majority of LDO systems.

Table 4.3: State-of-the-Art Comparison

Parameters	IEEE[15]	IEEE[20]	IEEE[27]	This Work
Technology (nm)	180	65	40	55
V_{DO}(mV)	200	300	200	200
V_{out}(V)	1.4	0.9	0.9	0.6
$I_{LOAD(max)}$(mA)	100	10	5	50
$C_{on-chip}$ (pF)	100	100	100	100
$I_Q(\mu A)$	49.64	28	233	22
ΔV_{out}(mV)	220.7	250	292	90
ΔI_{LOAD}(mA)	100	10	5	50
Line Reg (mV/V)	1.224	0.9	4.8	0.045
Load Reg (μV/mA)	40.7	12	37.9	1.4
Settling Time (μS)	1.26	1	0.354	0.1

Chapter 5

Conclusion

This thesis examines two fast transient, capacitor-less, LDO regulator prototype designs that was designed utilizing 55nm CMOS technology. The primary objective of the initial design is to improve the transient response characteristics while avoiding the requirement for a sizable off-chip capacitor.

In first LDO, the concept of using comparators for the purpose of enhancing transients in external capacitor-less LDO regulators has been effectively utilized. Comparators are used in order to facilitate the acceleration of the transient response of the regulator while simultaneously maintaining a low level of power consumption. The input voltage supplied is 1 volt, while the measured output voltage is 0.8 volts. The load fluctuates between 0 and 50 mA for a duration of 1 μs. Consequently, the CL-LDO produces an output voltage that experiences an overshoot of 33 mV and an undershoot of 34 mV, followed by a recovery time of 0.2 μs. A maximum of 26μA was allowed for the quiescent current. With a power consumption of only 90μW, the LDO can provide an output current of 1 mA and a dropout of 200 mV.

The second LDO design has a low quiescent current and a sizable pass transistor to improve the transient responsiveness. The experimental results indicate that the LDO2 regulator, equipped with a folded cascode EA circuit, operates with an I_Q of only 22μA and supplies a voltage of 0.8V-2V. It demonstrates an OS and US of 90mV, along with a recovery time of 0.1μs. The second LDO has a power consumption of 62μW. The target output voltage of 0.6V is successfully achieved. The analysis confirms the stability of the LDO regulator without requiring capacitors on the chip or off the chip, resulting in a satisfactory transient response with minimum overshoot and undershoot. Both LDOs that were designed successfully fulfill the specified

requirements, thus showcasing the capability to fabricate high performance LDOs with negligible quiescent current. The figure-of-merit (FoM) indicates that these low power LDOs have the capability to prolong the battery life of a range of applications.

$$FoM = T_S . \frac{I_Q}{I_{load(max)}} \tag{5.1}$$

Table 5.1: FoM

Parameter	IEEE[15]	IEEE[20]	IEEE[27]	[This Work]
FoM (ns)	0.625	2.8	16.4	0.044

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